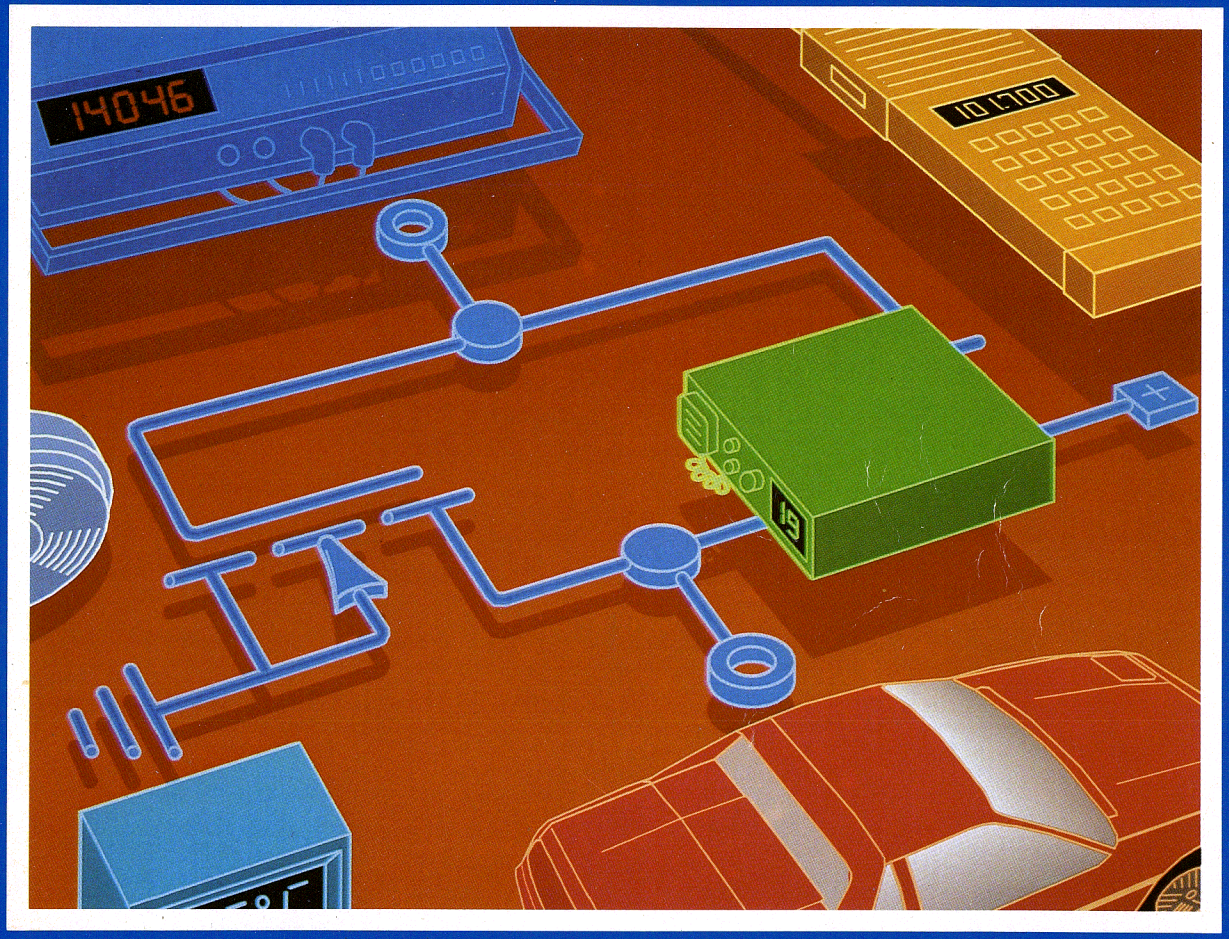
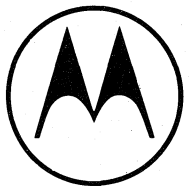
DL130

MOTOROLA



CMOS/NMOS SPECIAL FUNCTIONS DATA



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CMOS/NMOS SPECIAL FUNCTIONS DATA

Prepared by
Technical Information Center

This book presents technical data for the CMOS and NMOS Special Function integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a Function Selector Guide and a Handling Precautions chapter have been included to familiarize the user with these circuits.

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Master Index

1

MASTER INDEX

This index includes Motorola's entire MC14000 series CMOS products, although complete data sheets are included for only the Special Functions. Data sheets for devices in other books, are designated in the page number column as:

Logic — See DL131, CMOS Logic Data
Telecom — See DL136, Telecommunications Data
MCU — See DL132R1, Single-Chip Microcomputer Data
MPU — See DL133, 8-Bit Microprocessor and Peripheral Data

Handling and Design Guidelines

2

HANDLING AND DESIGN GUIDELINES

HANDLING PRECAUTIONS

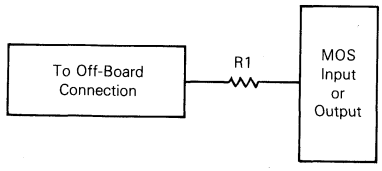
All MOS devices have an insulated gate that is subject to voltage breakdown. The gate oxide for Motorola's devices is about 800 Å thick and breaks down at a gate-source potential of about 100 V. The high-impedance gates on the devices are protected by resistor-diode networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Another effect of static damage is, often, increased leakage currents.

CMOS and NMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

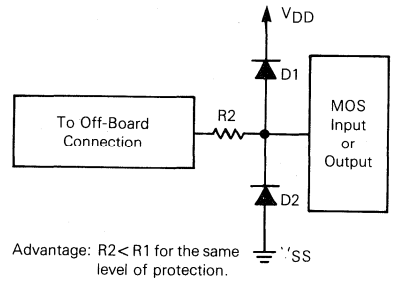
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS or NMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or NMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS or NMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS or NMOS devices should be stored or

FIGURE 1 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following:
A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 — PROPAGATION DELAY vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for the MC145040/1
k = 0.7 for other devices

EQUATION 2 — RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum rise time per data sheet in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for the MC145040/1
k = 2.3 for other devices

transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

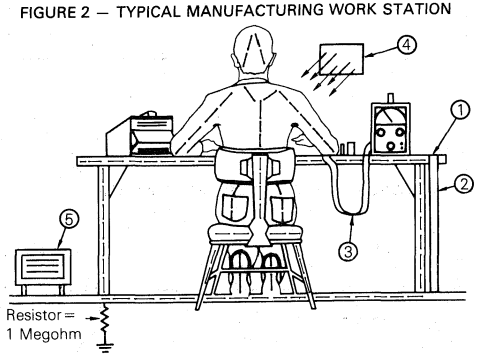
6. All CMOS or NMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS or NMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS or NMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS or NMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
17. Do not recycle shipping rails. Continuous use causes deterioration of their antistatic coating.

RECOMMENDED FOR READING

"Total Control of the Static in Your Business"

Available by writing to:
3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769-2963
Or by Calling:
1-800-328-1368

FIGURE 2 — TYPICAL MANUFACTURING WORK STATION



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than − 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:
   $-0.5 \le V_{in} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $-0.5 \le V_{out} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $|I_{in}| \le 10$ mA
   $|I_{out}| \le 10$ mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values. See Figure 1.
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of $I_{in} = 10$ mA. See Figure 1.
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 3 — CMOS WAFER CROSS SECTION

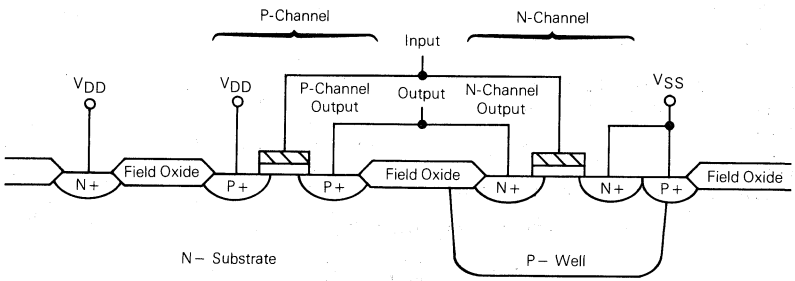
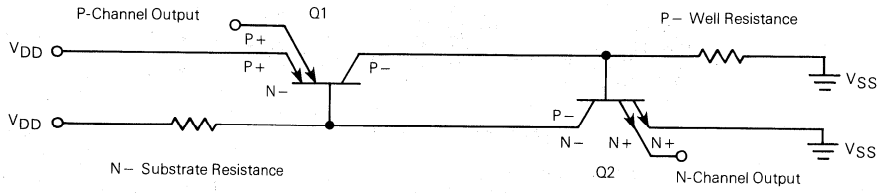


FIGURE 4 — LATCH UP CIRCUIT SCHEMATIC



CMOS ADCs/DACs

3

Device Number	Function
MC14433	3½ Digit A/D Converter
MC14435	Product Cancelled — See Other A/D Converters
MC14442	Microprocessor-Compatible A/D Converter
MC14443	6-Channel A/D Converter Subsystem
MC14444	Microprocessor-Compatible A/D Converter
MC14447	6-Channel A/D Converter Subsystem
MC14549B	Successive Approximation Register
MC14559B	Successive Approximation Register
MC144110	Digital-to-Analog Converter with Serial Interface
MC144111	Digital-to-Analog Converter with Serial Interface
MC145040	Analog-to-Digital Converter with Serial Interface
MC145041	Analog-to-Digital Converter with Serial Interface

Function	I/O Format	Resolution	Number of Analog Channels	On-Chip Oscillator	Other Features	Device Number	Number of Pins
ADC	Serial [Compatible with the Serial Peripheral Interface (SPI) on CMOS/NMOS MCUs]	8 Bits	11		Successive Approximation	**MC145040**	20
		8 Bits	11	✓	Successive Approximation	**MC145041**	20
	Parallel	3½ Digit BCD	1	✓	Dual Slope	**MC14433**	24
		8 Bits	11		Successive Approximation	**MC14442**	28
		8 Bits	15		Successive Approximation	**MC14444**	40
ADC Linear Subsystem	Parallel	8 to 10 Bits	6		Single Slope w/ Auto Zeroing	**MC14443**	16
		8 to 10 Bits	6		Single Slope w/ Auto Zeroing	**MC14447**	16
DAC	Serial [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	6 Bits	6		Emitter-Follower Outputs	**MC144110**	18
		6 Bits	4		Emitter-Follower Outputs	**MC144111**	14
Successive Approximation Register	Serial or Parallel	≤8 Bits			Cascadable for >8 Bits	**MC14549B**	16
		≤8 Bits			Cascadable for >8 Bits	**MC14559B**	16

MOTOROLA

MC14433

3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

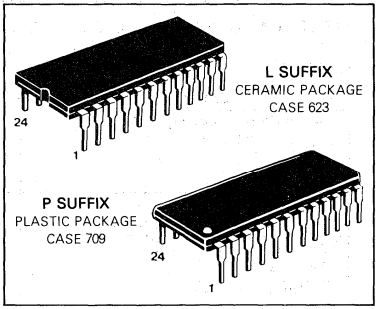
The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs – Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count
- See also Application Notes AN-769 and AN-770
- Chip Complexity: 1326 FETs

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

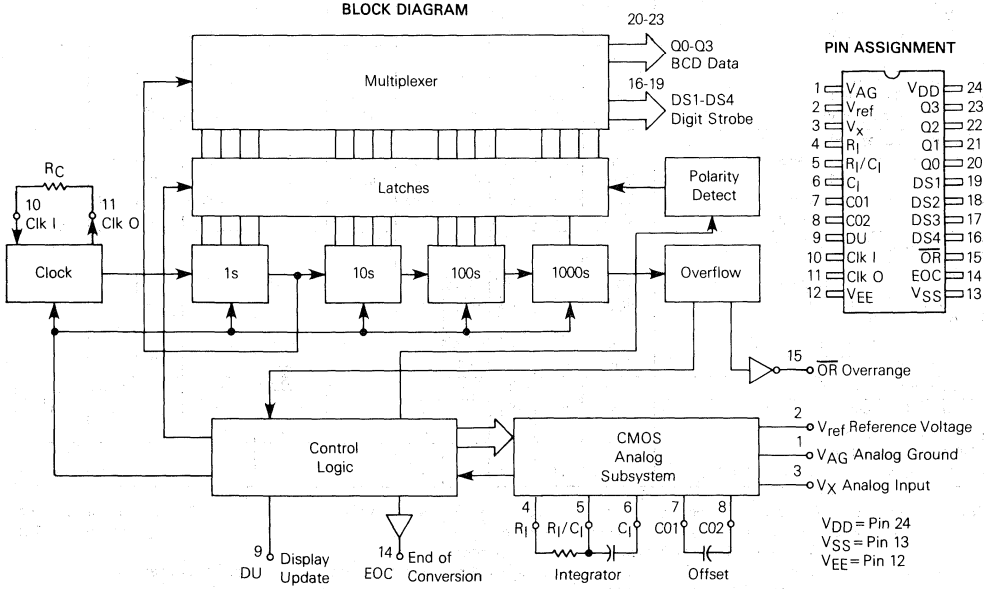
3½ DIGIT A/D CONVERTER



ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	−0.5 to +18	V
Voltage, any pin, referenced to V_{EE}	V	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	−2.8 to −8.0	
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_o	0.1 ± 20%	μF

ELECTRICAL CHARACTERISTICS (C_l = 0.1 μF mylar, R_l = 470 kΩ@V_{ref} = 2.000 V, R_l = 27 kΩ@V_{ref} = 200.0 mV, C_o = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1, unless otherwise indicated)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Linearity-Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	−5.0	–	–	−0.05 −1 Count	±0.05	+0.05 +1 Count	–	–	
(V_{ref} = 200.0 mV)		5.0	−5.0	–	–	–	±0.05	–	–	–	
Stability — Output Reading											
(V_X = 199.0 mV, V_{ref} = 200.0 mV)	–	5.0	−5.0					3★			LSD
Symmetry — Output Reading (Note 2)											
(V_{ref} = 2.000 V)	–	5.0	−5.0					4★			LSD
Zero-Output Reading											
(V_X = 0 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0	0	–	–	LSD
Bias Current — Analog Input	–	5.0	−5.0	–	–	–	±20	±100	–	–	pA
Reference Input		5.0	−5.0	–	–	–	±20	±100	–	–	
Analog Ground		5.0	−5.0	–	–	–	±20	±500	–	–	
Common Mode Rejection (f_{clk} = 32 kHz,											
V_X = 1.4 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	65	–	–	–	dB
Input Voltage* Pins 9, 10 "0" Level	V_{IL}										V
(V_O = 4.5 or 0.5 V)		5.0	–	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}										V
(V_O = 0.5 or 4.5 V)		5.0	–	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	–	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	–	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage — Pins 14 to 23											V
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	−5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	−5.0	–	4.95	–	
(V_{SS} = −5.0 V) "0" Level	V_{OL}	5.0	−5.0	–	4.95	–	−5.0	−4.95	–	−4.95	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current — Pins 14 to 23											mA
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	−5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	−5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = −5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	−5.0	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OL} = −4.5 V) Sink	I_{OL}	5.0	−5.0	1.6	–	1.3	2.25	–	0.9	–	
Input Current — DU, Pin 9	I_{DU}	5.0	−5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Quiescent Current	I_Q	5.0	−5.0	–	3.7	–	0.9	2.0	–	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	−8.0	–	7.4	–	1.8	4.0	–	3.2	
DC Supply Rejection											
(V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0.5	–	–	–	mV/V

Notes: 1. Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

2. Symmetry — Defined as the difference between a negative and positive reading of the same voltage at or near full scale.

★ Tighter tolerances are available. Consult Logic and Special Functions Product Marketing for details at (512) 928-6880.

* Referenced to V_{SS} for Pin 9. Referenced to V_{EE} for Pin 10.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

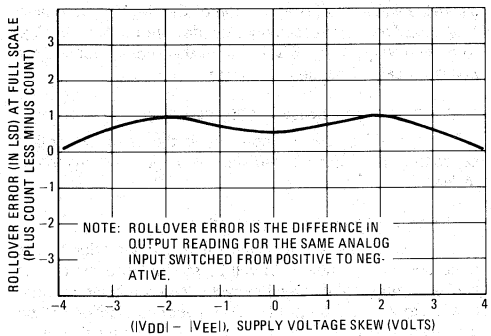


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

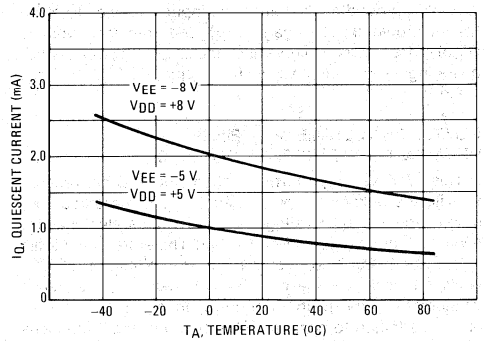


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

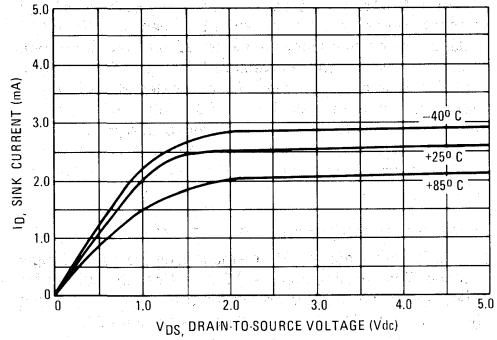


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

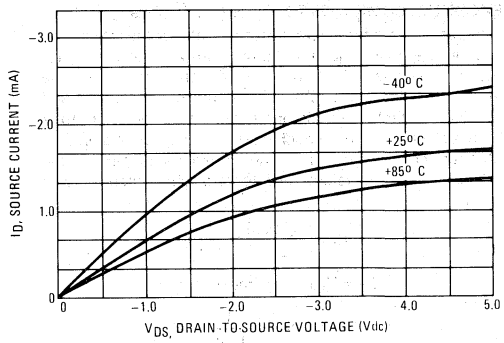


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

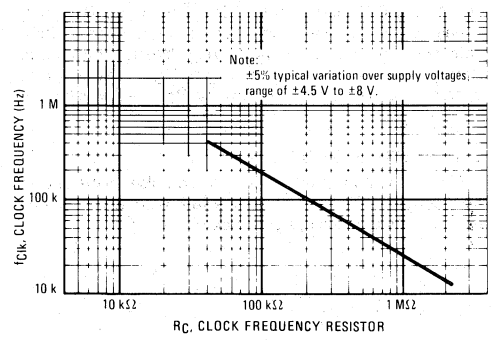
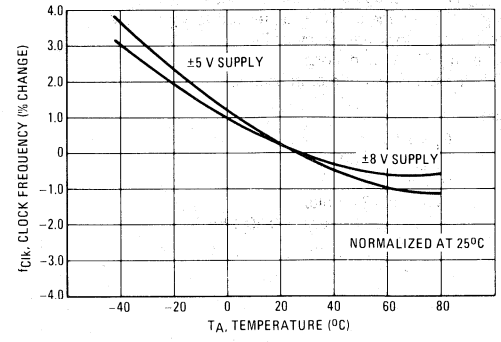


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$

PIN DESCRIPTIONS

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input. The allowable operating range for V_{AG} is from V_{EE} +2.8 V to V_{DD} −4.5 V.

REFERENCE VOLTAGE (V_{ref}, Pin 2) UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, Pin 2 functions as a reset for the A/D converter. When Pin 2 is switched low (referenced to V_{EE}) for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (polystyrene or mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(max) - 0.5\ V$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

R_I is in kΩ
V_{DD} is the voltage at Pin 24 referenced to V_{AG}
V_X is the voltage at Pin 3 referenced to V_{AG}, in V
f_{Clk} is the clock frequency at Pin 10 in kHz
C_I is in μF, ΔV is in Volts
T is the conversion time, in seconds

Example:

$C_I = 0.1\ \mu F$
$V_{DD} = 5.0$ volts
$f_{Clk} = 66$ kHz
For $V_X(max) = 2.0$ volts
$R_I = 480$ kΩ (use 470 kΩ ± 5%)
For $V_X(max) = 200$ mV
$R_I = 28$ kΩ (use 27 kΩ ± 5%)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow $\Delta V + V_X$ to exceed V_{DD}. The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (C01, C02; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF (polystyrene or mylar).

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (Pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, Pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through Pin 13. V_X-V_{EE} should be greater than 0.8 V.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY AND INPUT DU (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$) and the DU input. When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between V_{DD} −3.0 volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a positive pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (Pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select outputs and the EOC signal is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin. $V_{DD} - V_X$ should be greater than 2.5 V. $V_{DD} - V_{EE}$ should be greater than 7.8 V. V_{DD} determines V_{OH} for the digital outputs, and V_{IH} for the digital inputs.

TRUTH TABLE (DS1 = 1)

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table:
Q3 – ½ digit, low for "1", high for "0"
Q2 – Polarity: "1" = positive, "0" = negative
Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 – ALTERNATE OSCILLATOR CIRCUITS

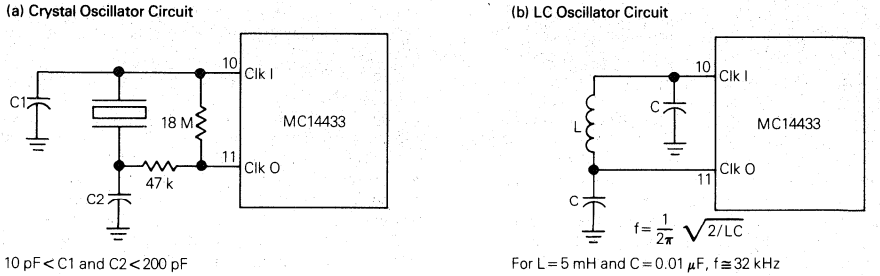


FIGURE 8 – DIGIT SELECT TIMING DIAGRAM

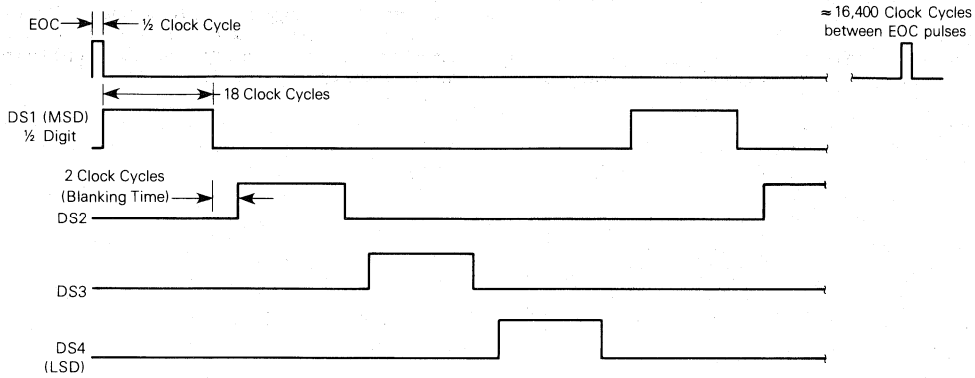


FIGURE 9 — INTEGRATOR WAVEFORMS AT PIN 6

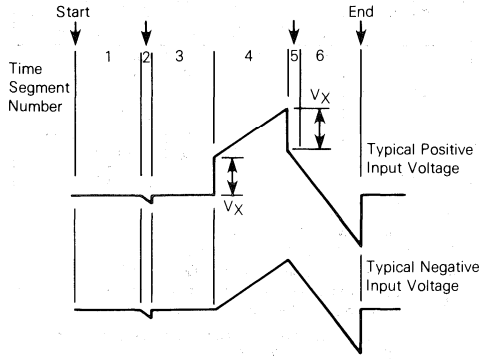
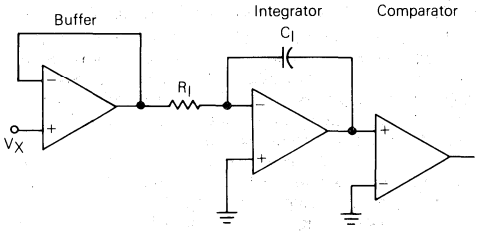


FIGURE 10 — EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 — The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

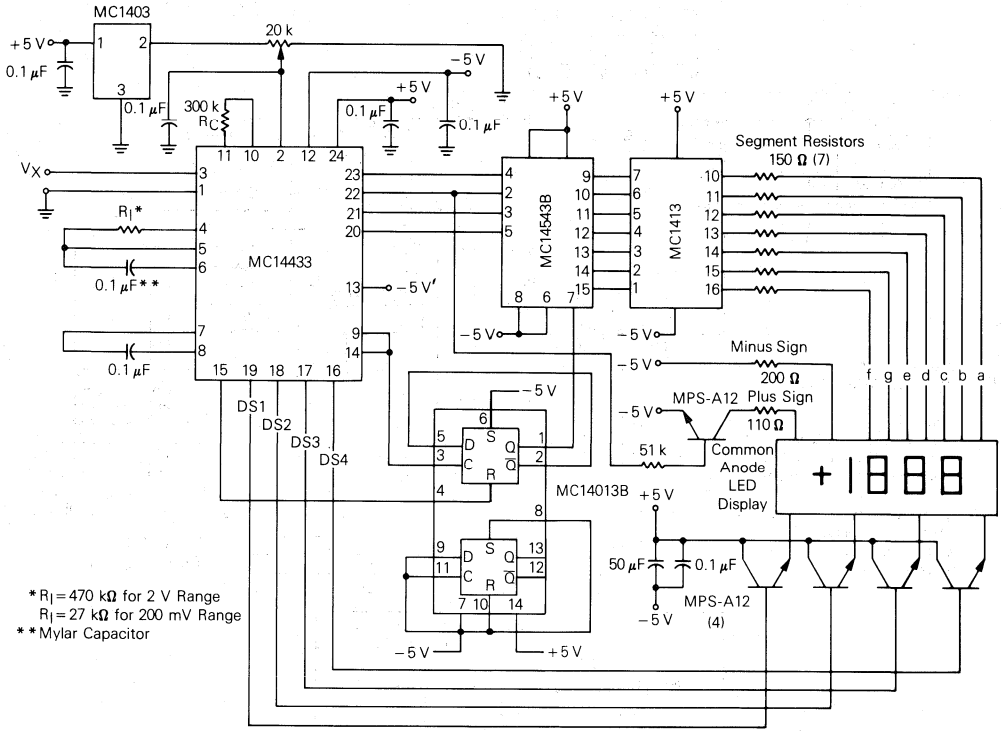
Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

FIGURE 11 — 3½ DIGIT VOLTMETER—COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

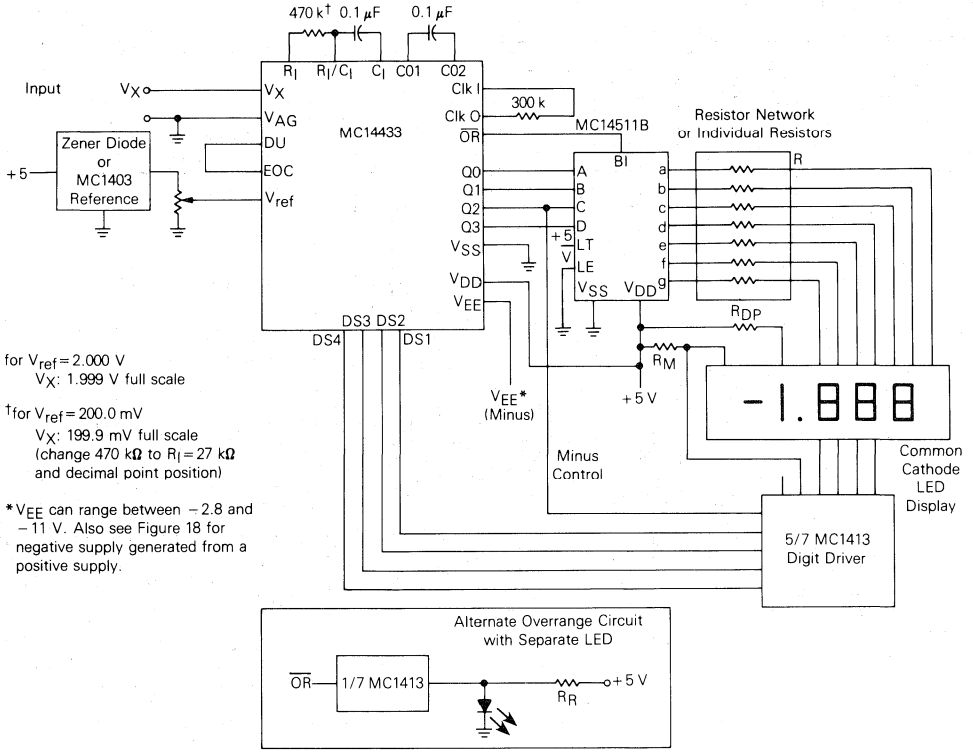
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and −5 V supplies is *not* required. See the recommended operating conditions and Figure 1.

FIGURE 12 – 3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT



for V_{ref} = 2.000 V
V_X: 1.999 V full scale

†for V_{ref} = 200.0 mV
V_X: 199.9 mV full scale
(change 470 kΩ to R_I = 27 kΩ and decimal point position)

*V_{EE} can range between −2.8 and −11 V. Also see Figure 18 for negative supply generated from a positive supply.

3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC1413 provides sink for digit current. (The MC1413 is a device with 7 Darlingtons with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP}. Since the brightness and the type and size of LED display are the choice of the designer, the values of resistors R, R_M, R_{DP}, and R_R that govern brightness are not given.

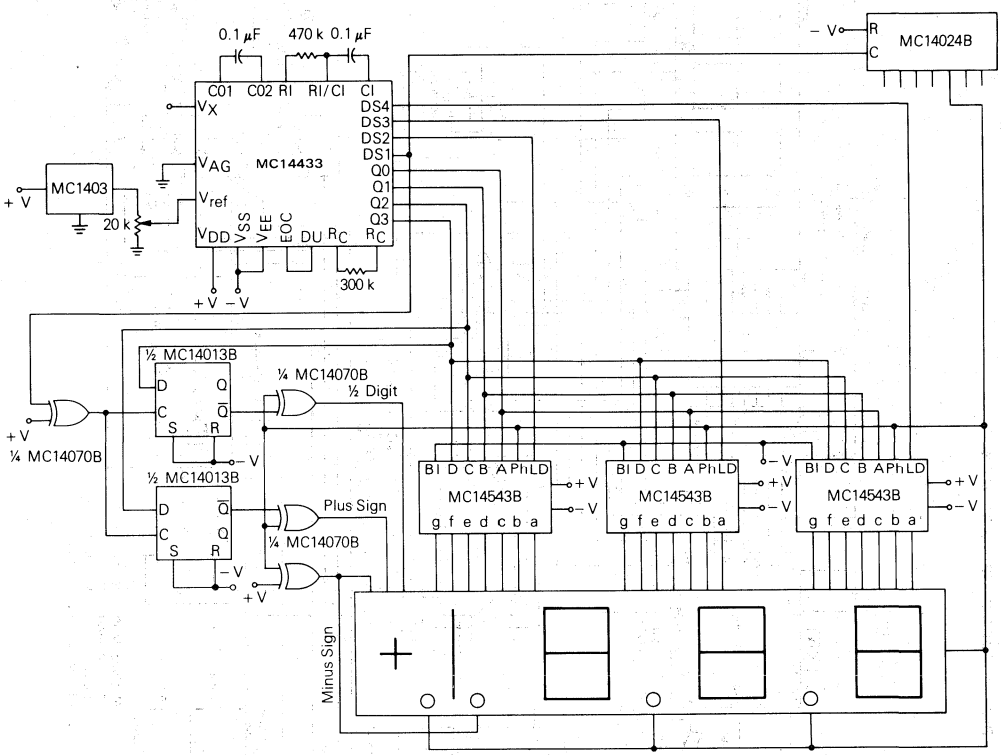
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of the LCD and to the individual segments through the combination of the output cir-

FIGURE 13 — 3½ DIGIT VOLTMETER WITH LCD DISPLAY



cuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE}. In this case a level must be set for analog ground, V_{AG}, which must be at least 2.8 V above V_{EE}. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE}, leaving 6 V for V_{DD} to V_{AG}. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 — TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY

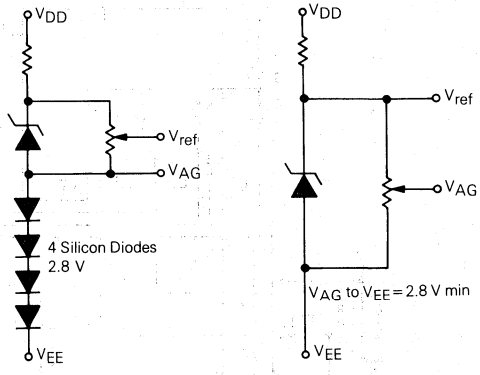
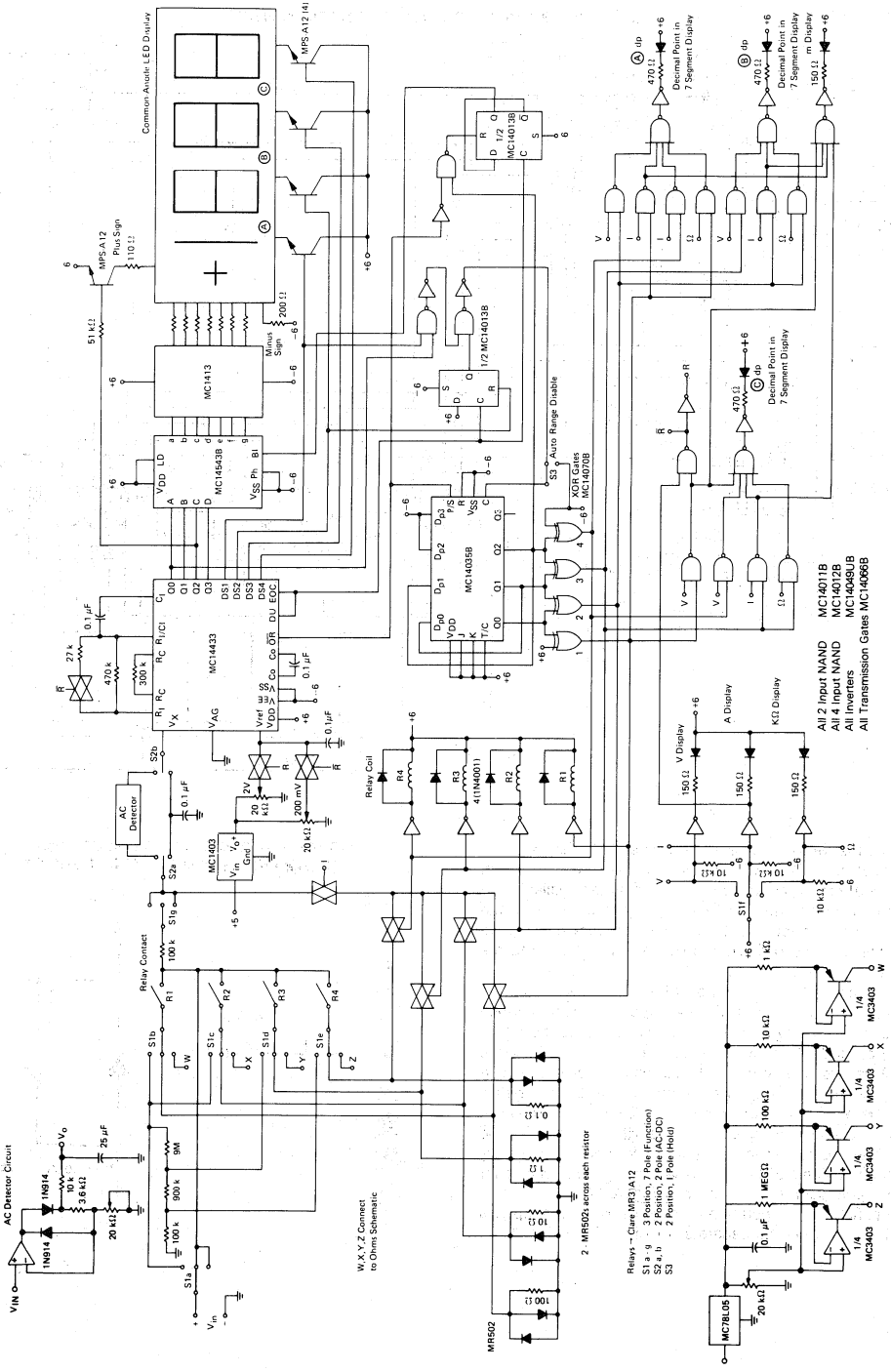


FIGURE 15 – 3½ DIGIT AUTORANGING MULTIMETER



3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 kΩ to 2 MΩ fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits. For additional information, see Motorola Application Note AN-769, "Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter."

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is V_{SS}. In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 — DEMULTIPLEXING FOR MC14433 BCD DATA

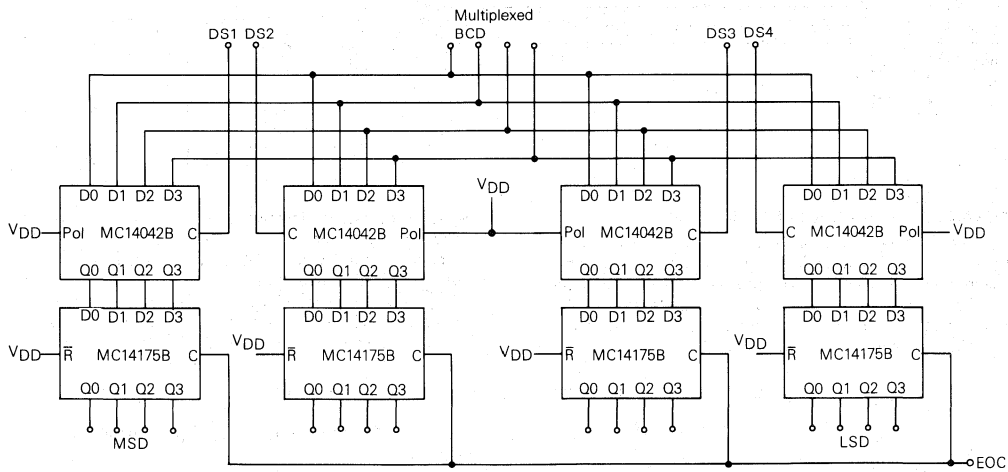
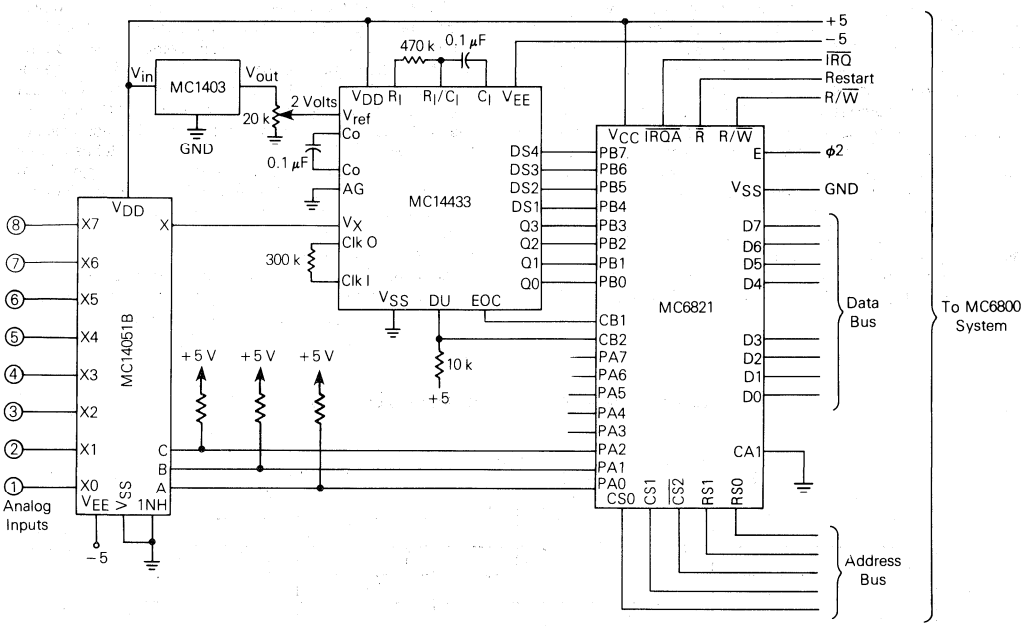


FIGURE 17 — CHANNEL DATA ACQUISITION HARDWARE

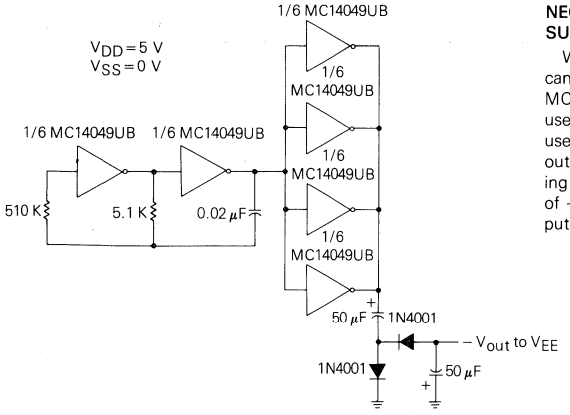


8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8-channel data acquisition network using the MC14433 and an MC6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6821 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

A more detailed explanation of this system including the actual software required for the M6800 microprocessor may be found in Motorola Application Note AN-770, "Data Acquisition Networks With NMOS and CMOS."

FIGURE 18 — NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049UB. Two inverters from CMOS hex inverter are used as an oscillator (≈3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a −4.3 V no load output voltage while the output with a 2 mA load is ≈3.4 V.

MOTOROLA

MC14435

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

The MC14435 A/D Logic is designed specifically for use in a dual-slope integration A/D converter system.

The device consists of 3-1/2 digits of BCD counters, 13 memory latches, and output multiplexing circuitry. An internal clock oscillator is provided to generate system timing and to set the output multiplexing rate. A single capacitor is required to set the oscillator frequency.

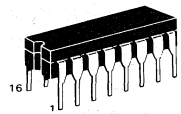
- On-Chip Clock to Control Digit Select, Multiplexing, and BCD Counters Simultaneously
- Multiplexed BCD Output
- Built-In 100-Count Delay for Accurate System Conversion of Low-Level Inputs
- System Over-Range Output
- Linear Companion Device Available From Motorola (MC1405L/1505L)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14435 EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14435EVL/VL/ VP)

CMOS LSI

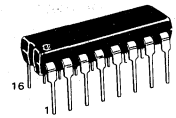
(LOW-POWER COMPLEMENTARY MOS)

3-1/2 DIGIT A/D LOGIC SUBSYSTEM

3



L SUFFIX
CERAMIC PACKAGE
CASE 620

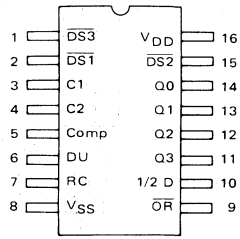


P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14435EFL/FL/FP – MC14435EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MC14435EFL/EVL MC14435FL/FP/VL/VP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



PRODUCT CANCELLED

Refer to Other A/D Converters Listed in the Function Selector Guide of This Book

MOTOROLA

MC14442

CMOS LSI

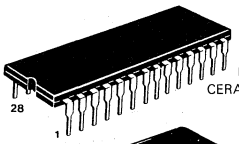
(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

MICROPROCESSOR-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER

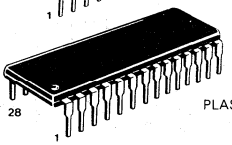
ANALOG-TO-DIGITAL CONVERTER (ADC)

The MC14442 ADC is a 28-pin bus-compatible 8-bit A/D converter with additional digital input capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles and allows up to 11 analog inputs. In addition, the part can accept up to 6 digital inputs. These inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control and bus interface is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at $f_E = 1.0$ MHz
- Ratiometric Conversion
- Completely Programmable
- Completely Software Compatible with the MC14444 ADC
- 5 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%



L SUFFIX
CERAMIC PACKAGE
CASE 733

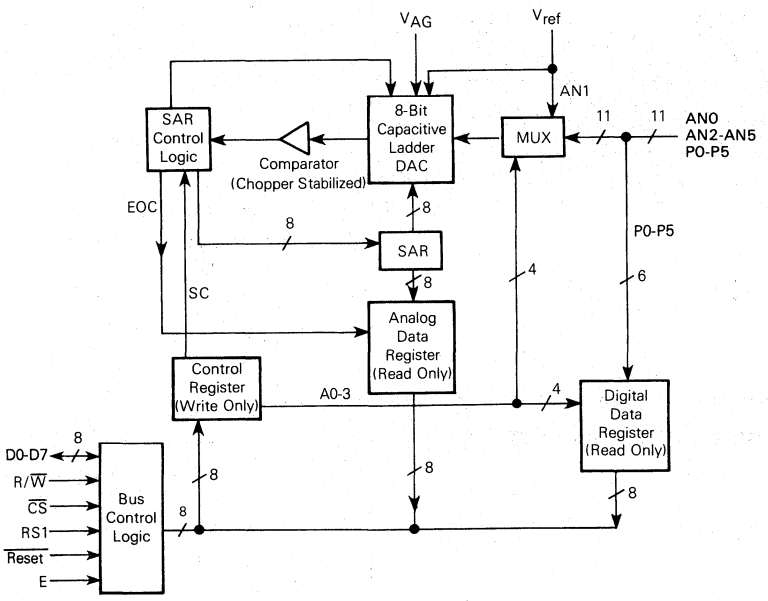


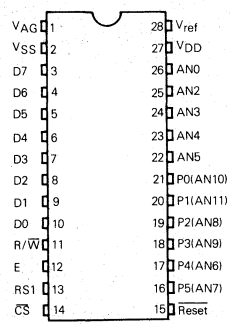
P SUFFIX
PLASTIC PACKAGE
CASE 710

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L — Ceramic Package
- P — Plastic Package

BLOCK DIAGRAM AND PIN ASSIGNMENT





MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.5	V
V_{in}	DC Input Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
V_{out}	DC Output Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±20	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: no derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 V ±10%, V_{SS}=0 V, T_A=−40°C to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS1, $\overline{CS}$)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5 V	–	±1	μA
Data Bus (D0-D7)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Three-State (Off State) Input Leakage Current	I_{TSI}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±10	μA
Output High Voltage	V_{OH}	I_{OH}=−1.6 mA	2.4	–	V
Output Low Voltage	V_{OL}	I_{OL}=1.6 mA	–	0.4	V
Peripheral Inputs (P0-P5)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±1.0	μA
Current Requirements					
Supply Current	I_{DD}	V_{DD}=5.5 V	–	10	mA
Input Current, V_{ref}	I_{ref}	V_{ref}=4.5 to 5.5 V	–	800	μA

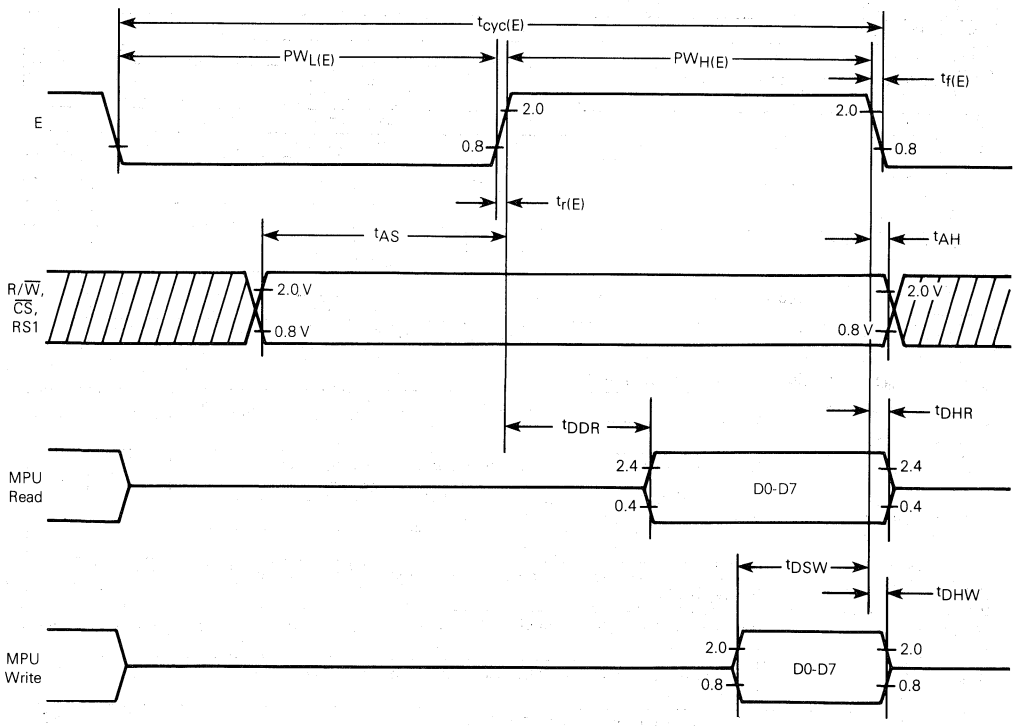
ANALOG CHARACTERISTICS (T_A=−40°C to 85°C)

Characteristic	Description	Min	Max	Unit
Analog Multiplexer				
Leakage Current	Leakage current between all deselected analog inputs and any selected analog input with all analog input voltages between V_{SS} and V_{DD}	–	±500	nA
A/D Converter (V_{SS}=0 V, V_{AG}=0 V, 4.5 V ≤ V_{ref} ≤ V_{DD} ≤ 5.5 V)				
Resolution	Number of bits resolved by the A/D	8	–	Bits
Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	–	± ½	LSB
Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	–	± ½	LSB
Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	–	± ½	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	–	± ½	LSB
Quantization Error	Uncertainty due to converter resolution	–	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	–	±1.0	LSB
Conversion Time	Total time to perform a single analog-to-digital conversion	–	32	E cycles
Sample Acquisition Time	Time required to sample the analog input	–	12	E cycles

AC CHARACTERISTICS ($T_A = -40°$ to $85°C$) (See Figure 1)

Characteristic	Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time ($1/f_E$)	E	$t_{cyc(E)}$	943	–	ns
Enable Clock Pulse Width, High	E	$PW_{H(E)}$	440	–	ns
Enable Clock Pulse Width, Low	E	$PW_{L(E)}$	410	–	ns
Clock Rise Time	E	$t_{r(E)}$	–	25	ns
Clock Fall Time	E	$t_{f(E)}$	–	30	ns
Address Setup Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AS}	145	–	ns
Data Delay (Read)	D0-D7	t_{DDR}	–	335	ns
Data Setup (Write)	D0-D7	t_{DSW}	185	–	ns
Address Hold Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AH}	10	–	ns
Input Data Hold Time	D0-D7	t_{DHW}	10	–	ns
Output Data Hold Time	D0-D7	t_{DHR}	10	–	ns
Input Capacitance	P0-P5, AN0-AN10,	C_{in}	–	55	pF
	R/$\overline{W}$, E, RS1, $\overline{CS}$, $\overline{RESET}$		–	15	
Three-State Output Capacitance	D0-D7	C_{out}	–	15	pF

FIGURE 1 – BUS TIMING



PIN FUNCTIONS

Pin No.	Pin Name	Function	Type
1	V_{AG}	A/D Converter Analog Ground	Supply
2	V_{SS}	Digital Ground	Supply
3	D7	Data Bus Bit 7 (MSB)	Input/Output
4	D6	Data Bus Bit 6	Input/Output
5	D5	Data Bus Bit 5	Input/Output
6	D4	Data Bus Bit 4	Input/Output
7	D3	Data Bus Bit 3	Input/Output
8	D2	Data Bus Bit 2	Input/Output
9	D1	Data Bus Bit 1	Input/Output
10	D0	Data Bus Bit 0 (LSB)	Input/Output
11	R/$\overline{W}$	Read/Write	Input
12	E	Enable Clock (ϕ2)	Input
13	RS1	Register Select	Input
14	$\overline{CS}$	Chip Select	Input
15	$\overline{Reset}$	Reset	Input
16	P5(AN7)	Digital Port or Analog Channel 7	Input
17	P4(AN6)	Digital Port or Analog Channel 6	Input
18	P3(AN9)	Digital Port or Analog Channel 9	Input
19	P2(AN8)	Digital Port or Analog Channel 8	Input
20	P1(AN11)	Digital Port or Analog Channel 11	Input
21	P0(AN10)	Digital Port or Analog Channel 10	Input
22	AN5	Analog Channel 5	Input
23	AN4	Analog Channel 4	Input
24	AN3	Analog Channel 3	Input
25	AN2	Analog Channel 2	Input
26	AN0	Analog Channel 0	Input
27	V_{DD}	Supply Voltage	Supply
28	V_{ref}	A/D Converter Positive Reference Voltage	Input

MC14442 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) — The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) — The enable clock provides two functions for the MC14442. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/$\overline{W}$) — The R/$\overline{W}$ signal is provided to the MC14442 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/$\overline{W}$ to transfer data out of either of the ADC data registers.

Reset ($\overline{Reset}$) — The reset line supplies the means of externally forcing the MC14442 into a known state. When a low is applied to the $\overline{Reset}$ pin, the start conversion bit of the control register is cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the $\overline{Reset}$ pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{CS}$) — Chip select is an active-low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{CS}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14442.

MC14442 ANALOG INPUTS AND DIGITAL INPUTS
(Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN5) — These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 12-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN6-AN11) — These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) – P0-P5 comprise a 6-bit digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

MC14442 SUPPLY VOLTAGE PINS

Positive Supply Voltage (V_{DD}) – V_{DD} is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14442 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (V_{SS}) – V_{SS} should be tied to system digital ground or the negative terminal of the V_{DD} power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high V_{SS} rejection.

Positive A/D Reference Voltage (V_{ref}) – This is the voltage used internally to provide references to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD}, but degradation of absolute A/D accuracy may result due to switching noise on V_{DD}.

A/D Ground Reference Voltage (V_{AG}) – This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

MC14442 INTERNAL REGISTERS

The MC14442 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

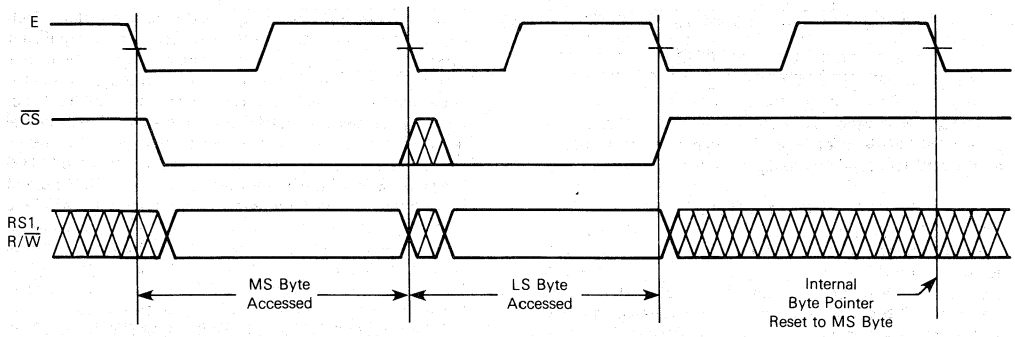
CAUTION: RS1 should **not** be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

INTERNAL REGISTER ADDRESSING

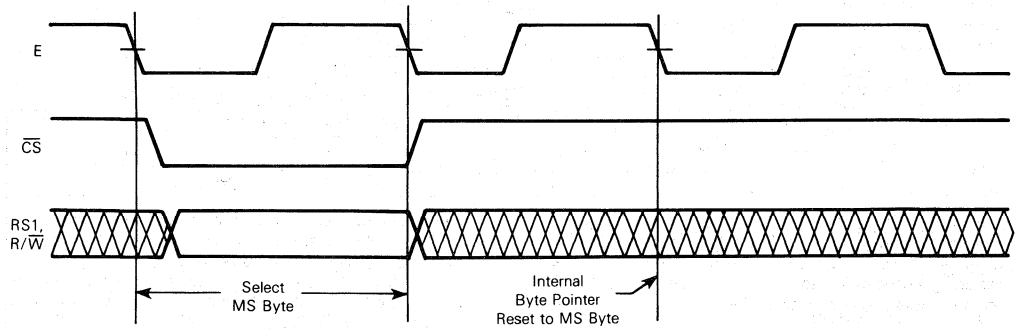
Addressing Signals				
$\overline{Reset}$	$\overline{CS}$	R/$\overline{W}$	RS1	ADC Response
0	X	X	X	Reset
1	0	0	0	No Response
1	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

FIGURE 2 — ADC ACCESS TIMING

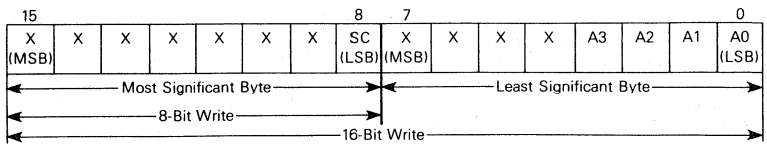
a — Typical 16-Bit ADC Access



b — Typical 8-Bit ADC Access



MC14442 CONTROL REGISTER
(Write Only)



Analog Multiplexer Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

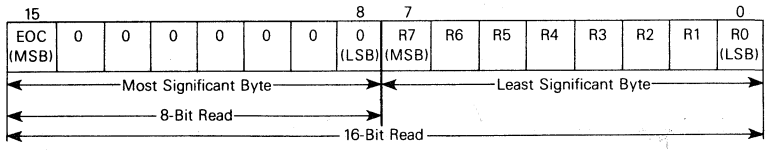
Hexadecimal Address (A3 = MSB)	Select
0	AN0
1	V_{ref}
2-5	AN2-AN5
6-B	AN6-AN11
C-F	Undefined

Start A/D Conversion (SC) – When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel will begin immediately after the completion of the control register write.

Unused Bits (X) – Bits 4-7 and 9-15 of the ADC Control Register are not used internally.

NOTE: A 16-bit control register write is required to change the analog multiplexer address. However, 8-bit writes to the MC14442 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

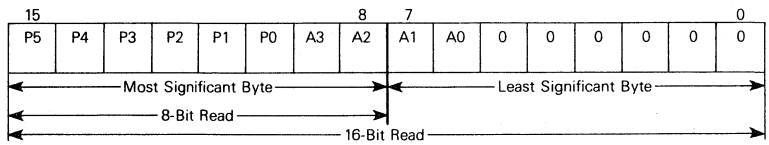
MC14442 ANALOG DATA REGISTER
(Read Only)



A/D Result (R0-R7) – The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of $FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) – The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14442 DIGITAL DATA REGISTER
(Read Only)



Logical Zero (0) – These bits are always read as logical zero.

Analog Multiplexer Address (A0-A3) – The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

ANALOG SUBSYSTEM
(See Block Diagram)

General Description

The analog subsystem of the MC14442 is composed of a 12-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of twelve channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as V_{DD} and V_{SS} power supply rejection.

Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14442 allows 2 enable clock cycles for the write into the control register even if only one byte is written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 KΩ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logic 0) if an A/D conversion is in progress.

FIGURE 3 — A/D TIMING SEQUENCE

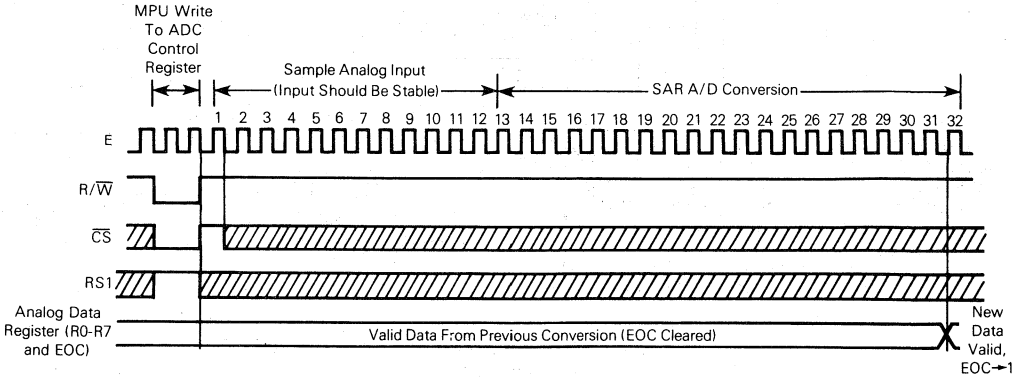
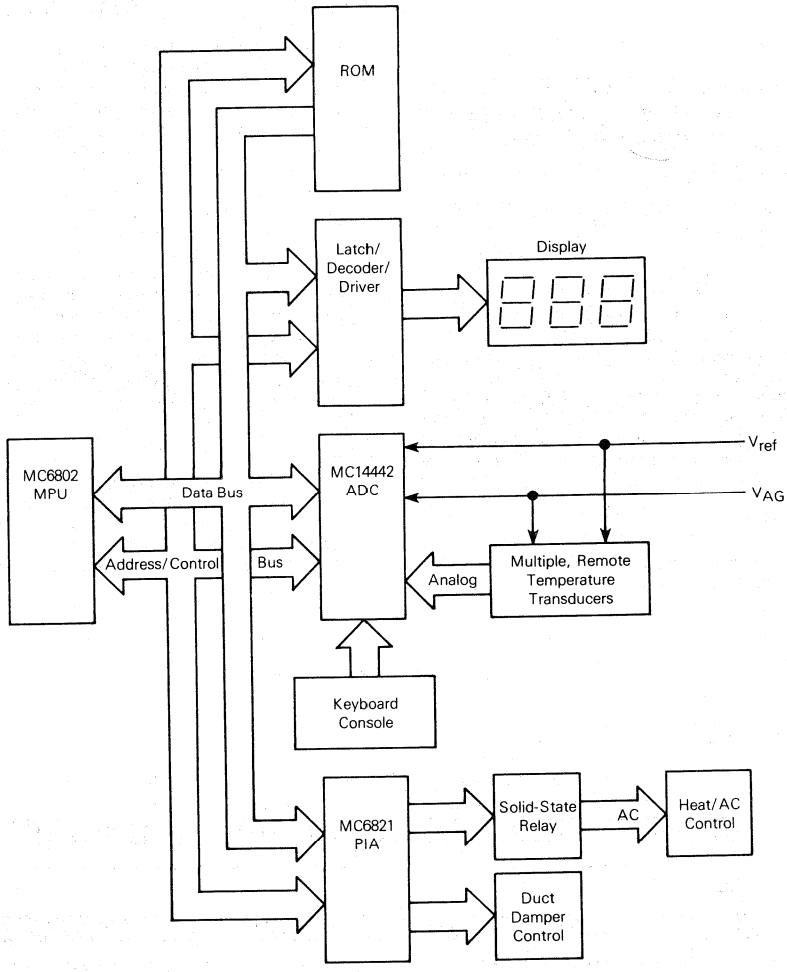


FIGURE 4 — TYPICAL MC14442 APPLICATION IN A CLIMATE CONTROLLER



MOTOROLA

MC14443
MC14447

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

MICROPROCESSOR-BASED ANALOG-TO-DIGITAL CONVERTER

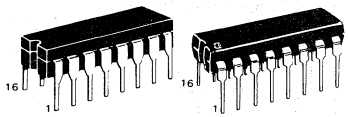
3

ANALOG-TO-DIGITAL CONVERTER LINEAR SUBSYSTEM

The MC14443 and the MC14447 are 6-channel, single-slope, 8-10 bit analog-to-digital converter linear subsystems for microprocessor-based data and control systems. Contained in both devices are a one-of-8 decoder, an 8-channel analog multiplexer, a buffer amplifier, a precision voltage-to-current converter, a ramp start circuit, and a comparator. The output driver of the MC14443's comparator is an open-drain N-channel which provides a sinking current. The output driver of the MC14447's comparator is a standard B-Series P-Channel, N-Channel pair.

A processor system (such as the MC141000 or MC146805) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog-to-digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at V_{DD} = 5 V
- Single Supply Operation +4.5 to +18 Volts
- Direct Interface to CMOS MPUs
- Typical Resolution — 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} − 2 V
- Chip Complexity: MC14443 — 150 FETs
  MC14447 — 151 FETs



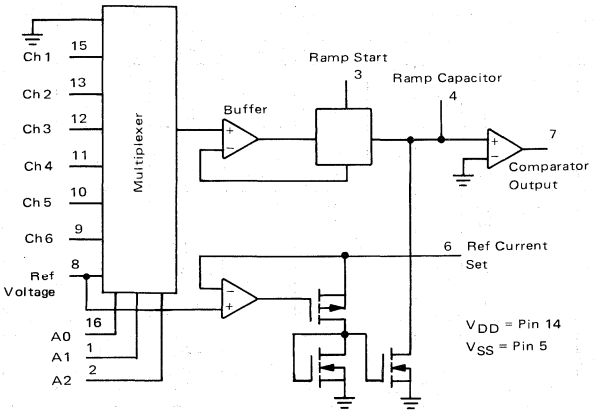
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

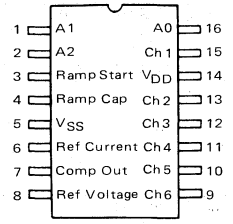
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Output Voltage—Comparator "0" Level	V_{OL}									V
V_{in} @ Pin 4 = 0 V		5.0	–	0.05	–	0.01	0.05	–	0.05	
		10	–	0.05	–	0.01	0.05	–	0.05	
		15	–	0.05	–	0.01	0.05	–	0.05	
V_{in} @ Pin 4 = 1.0 V "1" Level	V_{OH}									V
(R_{pullup} = 10 kΩ, MC14443 only)		5.0	4.95	–	4.95	4.99	–	4.95	–	
		10	9.95	–	9.95	9.99	–	9.95	–	
		15	14.95	–	14.95	14.99	–	14.95	–	
Input Voltage-Address, Ramp Start "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current—Comparator	I_{OH}									mA
V_{in} @ Pin 4 = 1.0 V (MC14447 only)										
(V_{OH} = 2.5 V)		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
V_{in} @ Pin 4 = 0 V	I_{OL}									mA
(V_{OL} = 0.4 V)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current—Address, Ramp Start	I_{in}	15	–	±0.3	–	–	±0.3	–	±1.0	μA
Input Current—Analog Inputs	I_{in}	15	–	–	–	±0.1	±50	–	–	nA
Input Capacitance—Address, Ramp Start V_{in} = 0 V	C_{in}	15	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5	–	–	–	0.8	1.5	–	–	mA
		10	–	–	–	1.5	–	–	–	
		15	–	–	–	1.7	3.0	–	–	
Crosstalk Between Any Two Input Channels	V_{Cr}	–	–	–	–	0	4.0	–	–	mV
Reference Current Range	I_R	–	–	–	10	–	50	–	–	μA
Channel Input Voltage Range	V_{AI}	5	–	–	0	–	3.0	–	–	V
		10	–	–	0	–	8.0	–	–	
		15	–	–	0	–	13.0	–	–	
Buffer Amplifier Output Offset	V_{BO}	5	–	–	–	0.285	–	–	–	V
		10	–	–	–	0.400	–	–	–	
		15	–	–	–	0.420	–	–	–	
Comparator Threshold	V_{TC}	5	–	–	0	0.195	V_{BO}	–	–	V
		10	–	–	0	0.275	V_{BO}	–	–	
		15	–	–	0	0.290	V_{BO}	–	–	
Reference Voltage Range	V_{ref}	5	–	–	2.0	–	3.0	–	–	V
		10			2.0		8.0	–	–	
		15	–	–	2.0	–	13.0	–	–	
Conversion Linearity	L_C									% Full
C > 100 pF, V_{AI} = 0 to 2.5 V, V_{ref} = 2.5 V		5	–	–	−0.5	–	+0.5	–	–	Scale
V_{AI} = 0 to 7.0 V, V_{ref} = 7.0 V		10	–	–	−0.5	–	+0.5	–	–	
V_{AI} = 0 to 12.0 V, V_{ref} = 12.0 V		15	–	–	−0.5	–	+0.5	–	–	

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Output Rise Time—Comparator (MC14447 only)	t_{TLH}	5.0	–	120	240	ns
		10	–	75	150	
		15	–	65	130	
Output Fall Time—Comparator	t_{THL}	5.0	–	250	500	ns
		10	–	350	700	
		15	–	650	1300	
Propagation Delay Time—Comparator MC14443 (R_L = 10 k to V_{DD})	t_{PLH}	5.0	–	550	1100	ns
		10	–	500	1000	
		15	–	550	1100	
	t_{PHL}	5.0	–	350	700	ns
		10	–	300	600	
		15	–	300	600	
MC14447	t_{PLH}	5.0	–	600	1200	ns
		10	–	475	950	
		15	–	500	1000	
	t_{PHL}	5.0	–	450	980	ns
		10	–	540	1080	
		15	–	750	1500	
Multiplexer Propagation Delay	t_M	5.0	–	180	360	ns
		10	–	125	250	
		15	–	110	220	
Ramp Start Delay Time	t_{TS}	5.0	–	40	80	ns
		10	–	25	50	
		15	–	20	40	
Acquisition Time* C = 1000 pF R_{ref} = 100 kΩ	t_A	5.0	–	30	60	μs
		10	–	15	30	
		15	–	14	28	

* Acquisition Time includes multiplexer propagation delay, ramp start propagation delay and the time required to charge ramp capacitor to the selected input voltage.

PIN DESCRIPTIONS

A2, A1, A0, ANALOG MUX ADDRESS INPUTS (PINS 2, 1, 16) — These inputs determine the input voltage source to be presented to the measurement system according to the Truth Table shown in Figure 2.

Ramp Start, RAMP START (PIN 3) — When Ramp Start is low, the ramp capacitor is charged to a voltage associated with the selected input channel. When Ramp Start is brought high, the connection to the input channel is broken and the capacitor begins to ramp toward V_{SS}. See Figure 4.

Ramp Cap, RAMP CAPACITOR (PIN 4) — The ramp capacitor is used to generate a time period when discharged from a selected voltage via a precise reference current. A polystyrene or mylar capacitor is recommended. The value should be ≥ 100 pF so that the board and stray capacitances have negligible effects. Large values of capacitance with the associated large leakage currents are not recommended because the leakage current must be insignificant in comparison to the minimum reference current (10 μA).

V_{SS}, NEGATIVE POWER SUPPLY (PIN 5) — This is system ground.

Ref Current, REFERENCE CURRENT (PIN 6) — To discharge the ramp capacitor, the reference current is fixed via a resistor (R_{ref}) to a positive supply from Pin 6. Typical current is equal to $(V_{DD} - V_{ref})/R_{ref}$.

Comp Out, COMPARATOR OUTPUT (PIN 7) — This output is low when the capacitor has reached the discharged voltage and is high otherwise. The MC14443 requires a pull-up resistor on Pin 7 due to the open-drain configuration. The MC14447 does not require a pull-up resistor.

Ref Voltage, REFERENCE VOLTAGE (PIN 8) — This is the known voltage to which the unknown is compared.

INPUT CHANNELS (PINS 9, 10, 11, 12, 13, 15) — Input channels 1 through 6 are used to monitor up to six separate unknown voltages. Selection is via the address inputs.

V_{DD}, POSITIVE POWER SUPPLY (PIN 14) — This pin is the package positive power supply pin.

FIGURE 1 – VOLTAGE TO PULSE WIDTH CONVERSION

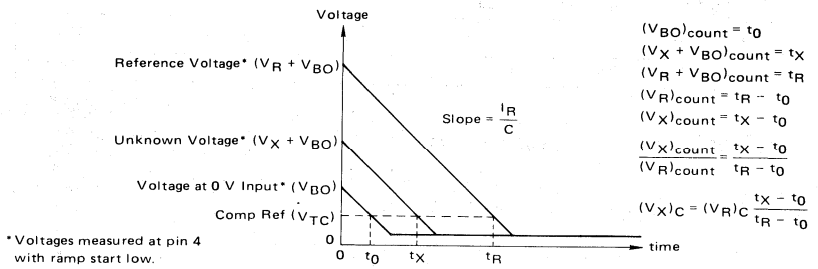


FIGURE 2 – TRUTH TABLE

A2	A1	A0	Input Selected	
0	0	0	V_{SS}	Channel 0 (ground)
0	0	1	Ch1	Channel 1
0	1	0	Ch2	Channel 2
0	1	1	Ch3	Channel 3
1	0	0	Ch4	Channel 4
1	0	1	Ch5	Channel 5
1	1	0	Ch6	Channel 6
1	1	1	V_{ref}	Channel 7 (External Reference)

FIGURE 3 – TYPICAL APPLICATIONS CIRCUIT

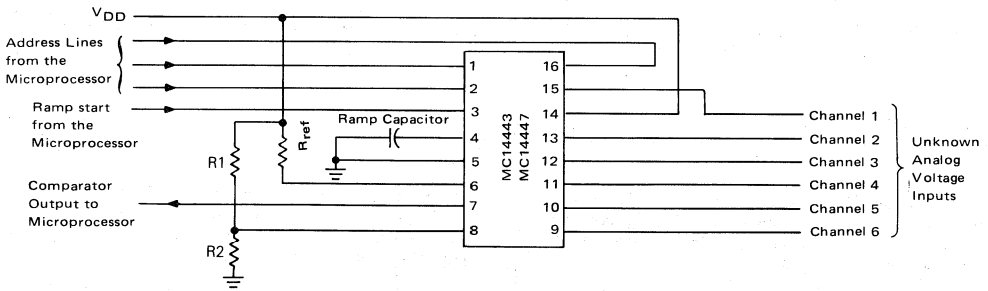


FIGURE 4 – SOFTWARE FLOW (CONVERSION SEQUENCE)

Step No.	A2	A1	A0	Ramp Start	Comment
1.	1	1	1	0	Channel 7 Selected (Reference Voltage)
2.	1	1	1	1	Record time until Pin 7 goes low
3.	0	0	0	0	Channel 0 Selected (Ground)
4.	0	0	0	1	Record time until Pin 7 goes low
5.	0	0	1	0	Channel 1 Selected
6.	0	0	1	1	Record time until Pin 7 goes low
Calculate $t_{Ch7} - t_{Ch0} = t_{Ch7'}$ Step 2–Step 4					
Calculate $t_{Ch1} - t_{Ch0} = t_{Ch1'}$ Step 6–Step 4					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch1'}/t_{Ch7'})$*					
7.	0	1	0	0	Channel 2 Selected
8.	0	1	0	1	Record time until Pin 7 goes low
Calculate $t_{Ch2} - t_{Ch0} = t_{Ch2'}$					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch2'}/t_{Ch7'})$†					
etc.					

*Weighting of the analog signal on Channel 1.
†Weighting of the analog signal on Channel 2.

MOTOROLA

MC14444

CMOS LSI

(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

MICROPROCESSOR-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER

3

ANALOG-TO-DIGITAL CONVERTER (ADC)

The MC14444 ADC is a 40-pin bus-compatible 8-bit A/D converter with additional digital I/O capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles at 1 MHz and allows for up to 15 analog inputs. In addition, the part has a 3-bit digital I/O port and can accept up to 9 digital inputs. Six of these inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control, bus interface and maskable interrupt capability is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at f_E = 1.0 MHz
- Ratiometric Conversion
- Completely Programmable
- Polled or Interrupt Driven Operation
- 3 Dedicated Digital Inputs
- 3-Bit Digital I/O Port
- 9 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%

P SUFFIX
PLASTIC PACKAGE
CASE 711

L SUFFIX
CERAMIC PACKAGE
CASE 734

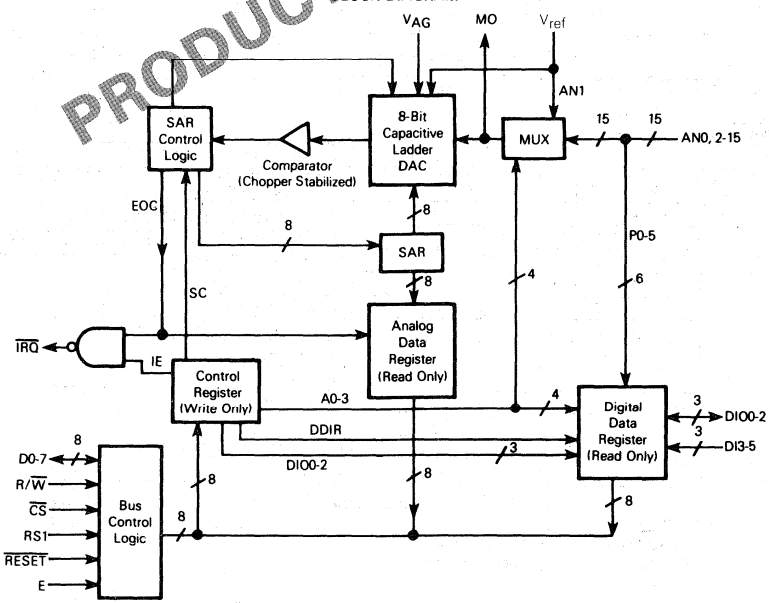
ORDERING INFORMATION

MC14XXX

L	Ceramic Package
P	Plastic Package

Suffix Denotes

BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.5	V
V_{in}	DC Input Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
V_{out}	DC Output Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±20	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: no derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 V ±10%, V_{SS}=0 V, T_A= −40° to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS1, $\overline{CS}$)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5 V	–	+1	μA
Interrupt Output ($\overline{IRQ}$)					
Output Low Voltage	V_{OL}	I_{Load}=1.6 mA	–	0.4	V
Output Leakage Current (Off State)	I_{LOH}	$V_{OH}=V_{DD}$=5.5 V	–	10	μA
Data Bus (D0-D7)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Three-State (Off State) Input Leakage Current	I_{TSI}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±10	μA
Peripheral I/O (DIO0-DIO2, DI3-DI5, P0-P5)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current DI3-DI5, P0-P5	I_{in}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±1.0	μA
Output High Voltage DIO0-DIO2	V_{OH}	I_{OH}=−0.19 mA	V_{DD}−0.4	–	V
Output Low Voltage DIO0-DIO2	V_{OL}	I_{OL}=0.975 mA	–	0.4	V
Three-State (Off State) Input Leakage Current DIO0-DIO2	I_{TSI}	V_{DD}=5.5 V, $V_{SS} \le V_{out} \le V_{DD}$	–	±10	μA
Current Requirements					
Supply Current	I_{DD}	V_{DD}=5.5 V, f_E=1 MHz	–	10	mA
Converter Input Current	I_{ADC}	Analog input current at f_E=1 MHz with multiplexer inputs between V_{SS} and V_{DD}	–	±500	nA
Reference Input Current V_{ref}	I_{ref}	V_{ref}=4.5 to 5.5 V	–	800	μA

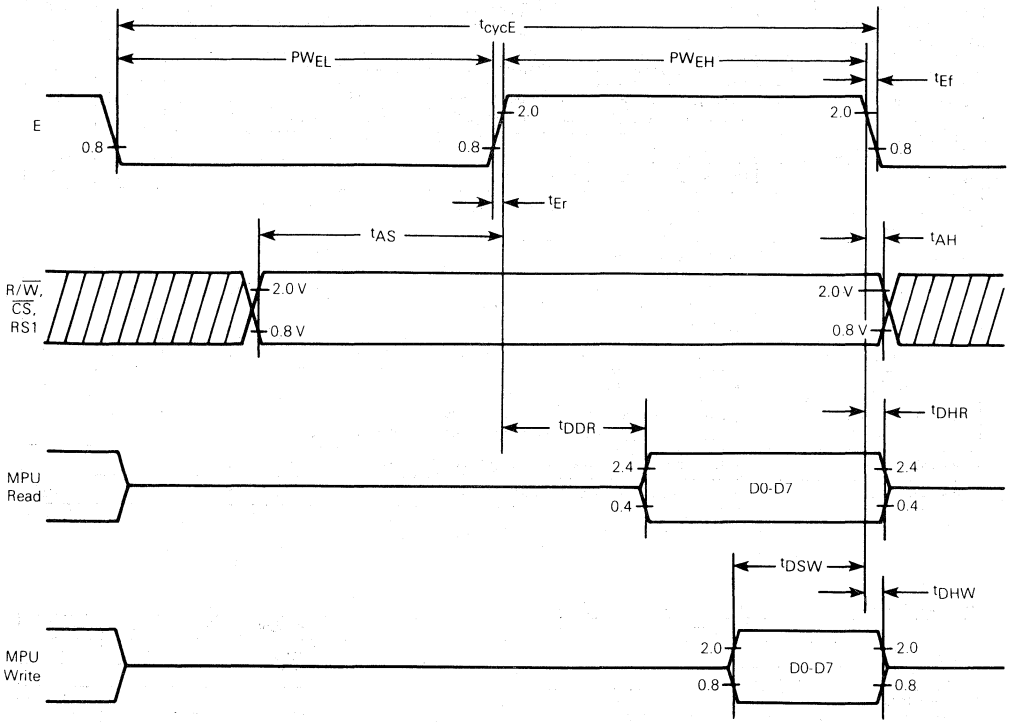
ANALOG CHARACTERISTICS ($T_A = -40°C$ to $85°C$)

Characteristic	Description	Min	Max	Unit
Analog Multiplexer				
On Resistance	Resistance between each analog input and multiplexer output	–	5	kΩ
Leakage Current	Leakage current between all deselected analog inputs and any selected analog input with all analog input voltages between V_{SS} and V_{DD}	–	±400	nA
A/D Converter ($V_{SS}=0$ V, $V_{AG}=0$ V, 4.5 V ≤ V_{ref} ≤ V_{DD})				
Resolution	Number of bits resolved by the A/D	8	–	Bits
Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	–	± ½	LSB
Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	–	± ½	LSB
Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	–	± ½	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	–	± ½	LSB
Quantization Error	Uncertainty due to converter resolution	–	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	–	± 1.0	LSB
Conversion Time	Total time to perform a single analog-to-digital conversion	–	32	E cycles
Sample Acquisition Time	Time required to sample the analog input	–	12	E cycles

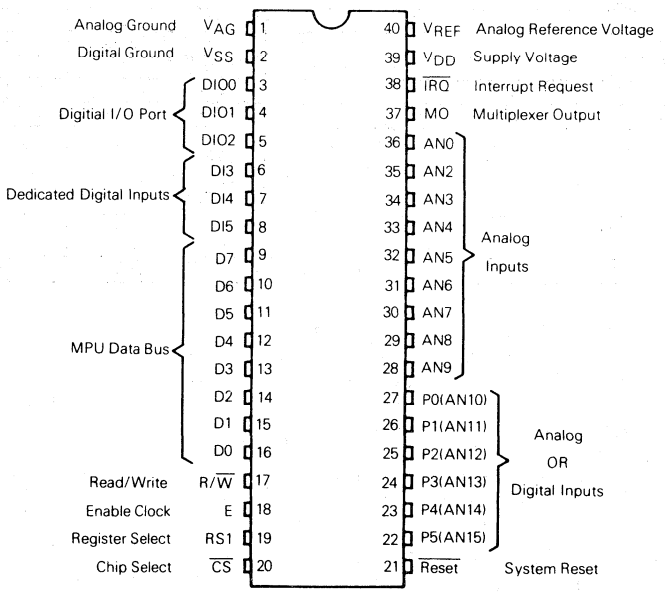
AC CHARACTERISTICS ($T_A = -40°$ to $85°C$) (See Figure 1)

Characteristic	Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time ($1/f_E$)	E	t_{cycE}	943	–	ns
Enable Clock Pulse Width, High	E	PW_{EH}	440	–	ns
Enable Clock Pulse Width, Low	E	PW_{EL}	410	–	ns
Clock Rise Time	E	t_{Er}	–	25	ns
Clock Fall Time	E	t_{Ef}	–	30	ns
Address Setup Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AS}	145	–	ns
Data Delay (READ)	D0-D7	t_{DDR}	–	335	ns
Data Setup (WRITE)	D0-D7	t_{DSW}	185	–	ns
Address Hold Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AH}	10	–	ns
Input Data Hold Time	D0-D7	t_{DHW}	10	–	ns
Output Data Hold Time	D0-D7	t_{DHR}	10	–	ns
Input Capacitance	AN0-AN15	C_{in}	–	55	pF
	DI0-DI5, R/$\overline{W}$, E, RS1, $\overline{CS}$, $\overline{RESET}$		–	15	
Three-State Output Capacitance	DIO0-DIO2 D0-D7	C_{out}	–	15	pF
High-Impedance Output Capacitance	$\overline{IRQ}$	C_{out}	–	15	pF

FIGURE 1 – BUS TIMING



PIN ASSIGNMENT



PIN FUNCTIONS

Pin No.	Pin Name	Function	Type
1	V_{AG}	A/D Converter Analog Ground	Supply
2	V_{SS}	Digital Ground	Supply
3	DIO0	Digital Port	Input/Output
4	DIO1	Digital Port	Input/Output
5	DIO2	Digital Port	Input/Output
6	DI3	Digital Port	Input
7	DI4	Digital Port	Input
8	DI5	Digital Port	Input
9	D7	Data Bus Bit 7 (MSB)	Input/Output
10	D6	Data Bus Bit 6	Input/Output
11	D5	Data Bus Bit 5	Input/Output
12	D4	Data Bus Bit 4	Input/Output
13	D3	Data Bus Bit 3	Input/Output
14	D2	Data Bus Bit 2	Input/Output
15	D1	Data Bus Bit 1	Input/Output
16	D0	Data Bus Bit 0 (LSB)	Input/Output
17	R/$\overline{W}$	Read/Write	Input
18	E	Enable Clock (ϕ2)	Input
19	RS1	Register Select	Input
20	$\overline{CS}$	Chip Select	Input
21	$\overline{Reset}$	Reset	Input
22	P5(AN15)	Digital Port or Analog Channel 15	Input
23	P4(AN14)	Digital Port or Analog Channel 14	Input
24	P3(AN13)	Digital Port or Analog Channel 13	Input
25	P2(AN12)	Digital Port or Analog Channel 12	Input
26	P1(AN11)	Digital Port or Analog Channel 11	Input
27	P0(AN10)	Digital Port or Analog Channel 10	Input
28	AN9	Analog Channel 9	Input
29	AN8	Analog Channel 8	Input
30	AN7	Analog Channel 7	Input
31	AN6	Analog Channel 6	Input
32	AN5	Analog Channel 5	Input
33	AN4	Analog Channel 4	Input
34	AN3	Analog Channel 3	Input
35	AN2	Analog Channel 2	Input
36	AN0	Analog Channel 0	Input
37	MO	Analog Multiplexer Output	Test Only
38	$\overline{IRQ}$	Interrupt Request	Open-Drain Output
39	V_{DD}	Supply Voltage	Supply
40	V_{ref}	A/D Converter Positive Reference Voltage	Input

MC14444 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) — The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) — The enable clock provides two functions for the MC14444. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/$\overline{W}$) — The R/$\overline{W}$ signal is provided to the MC14444 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/$\overline{W}$ to transfer data out of either of the ADC data registers.

Reset ($\overline{RESET}$) — The reset line supplies the means of externally forcing the MC14444 into a known state. When a low is applied to the $\overline{RESET}$ pin, the start conversion, interrupt enable and I/O port data direction bits of the control register are cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus and I/O port output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the $\overline{RESET}$ pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{CS}$) — Chip select is an active-low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{CS}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14444.

MC14444 ANALOG INPUTS AND DIGITAL I/O
(Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN9) — These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 16-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN10-AN15) — These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) — P0-P5 comprise a 6-bit digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

> **CAUTION:** Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

Digital I/O Port (DIO0-DIO2) — These pins serve as a 3-bit digital I/O port. At reset the port is configured as an input and may be read from the ADC digital data register. The port may be programmed as an output by setting the DDIR bit in the control register to a logical 1. See the control register discussion for further details. When configured as an output, the DIO port will provide CMOS logic levels for limited dc load currents. (Refer to the Electrical Specifications for the dc drive capability of this port.) New output states are transferred to the external pins on the last falling edge of E during a 16-bit write to the control register. When configured as an input, the port will accept both TTL and CMOS logic levels.

Dedicated Digital Inputs (DI3-DI5) — These three pins are dedicated as digital inputs whose values may be read from the ADC digital data register. They are also TTL and CMOS compatible.

MC14444 SUPPLY VOLTAGE PINS AND TEST PIN

Positive Supply Voltage (V_{DD}) — V_{DD} is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14444 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (V_{SS}) — V_{SS} should be tied to system digital ground or the negative terminal of the V_{DD} power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high V_{SS} rejection.

Positive A/D Reference Voltage (V_{ref}) — This is the voltage used internally to provide references to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD}, but degradation of absolute A/D accuracy may result due to switching noise on V_{DD}.

A/D Ground Reference Voltage (V_{AG}) — This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

Multiplexer Output (MO) — The analog multiplexer selects one of 16 analog input channels and connects it to the input of the A/D converter. The multiplexer output is internally connected to the A/D input and requires no external jumpers. Since loading of the MO pin affects the charging time of the DAC, **it is recommended that no connection be made to the MO pin.**

MC14444 INTERNAL REGISTERS

The MC14444 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

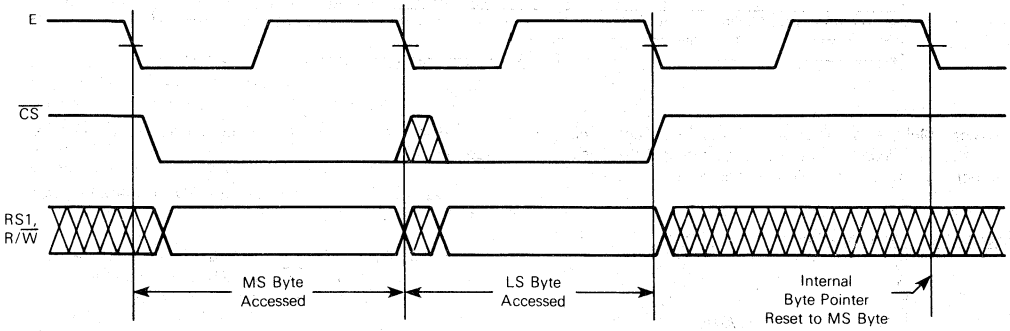
> **CAUTION:** RS1 should not be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

INTERNAL REGISTER ADDRESSING

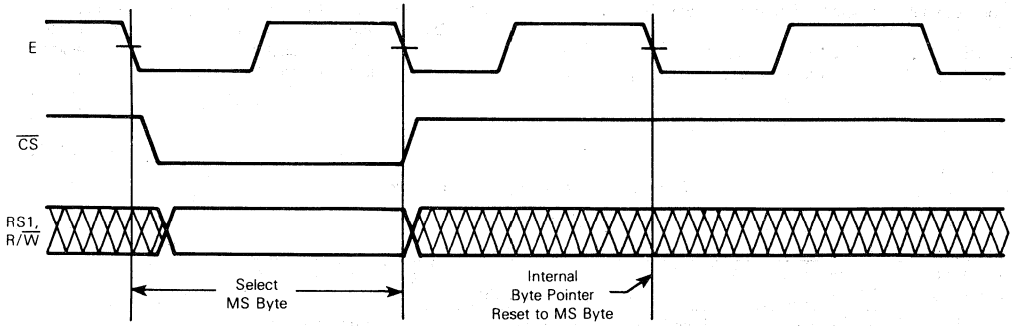
Addressing Signals				ADC Response
$\overline{RESET}$	$\overline{CS}$	R/$\overline{W}$	RS1	
0	X	X	X	Reset
1	0	0	0	No Response
1	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

FIGURE 2 — ADC ACCESS TIMING

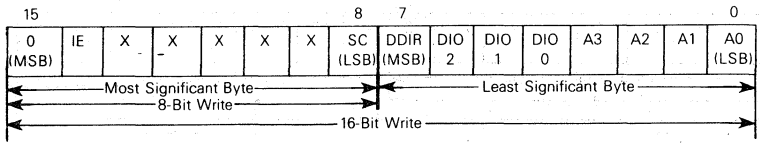
a — Typical 16-Bit ADC Access



b — Typical 8-Bit ADC Access



MC14444 CONTROL REGISTER
(Write Only)



Analog Multiplexer Address (A0-A3) — These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

Hexadecimal Address (A3 = MSB)	Select
0	AN0
1	V_{REF}
2-9	AN2-AN9
A-F	AN10-AN15(P0-P5)

Digital I/O Output (DIO0-DIO2) — When the MPU configures the 3-bit I/O port as an output, these are the bit locations into which the output states are written.

I/O Port Data Direction (DDIR) — This is the data direction bit for the 3-bit I/O port. A logical 1 configures the port as output while a logical 0 configures the port as input.

Start A/D Conversion (SC) — When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel will begin immediately after the completion of the control register write.

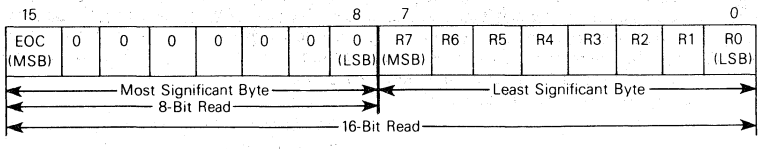
Unused Bits (X) — Bits 9-13 of the ADC Control Register are not used internally.

Interrupt Enable (IE) — The interrupt enable bit, when set to a logical 1, allows the $\overline{IRQ}$ pin to be activated at the completion of the next analog to digital conversion.

Control Register MSB — The MSB of the most significant byte of the ADC control register must be written as a logical 0.

NOTE: A 16-bit control register write is required to change the analog multiplexer address or to update the DIO port. However, 8-bit writes to the MC14444 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

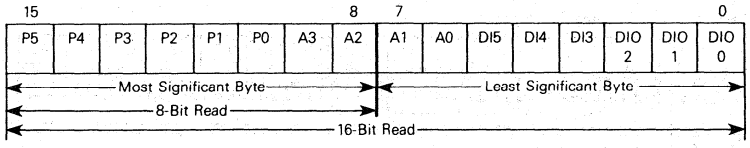
MC14444 ANALOG DATA REGISTER
(Read Only)



A/D Result (R0-R7) — The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of $FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) — The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single 8-bit M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14444 DIGITAL DATA REGISTER
(Read Only)



Digital I/O Port (DIO0-DIO2) — The states of the three digital I/O pins are read from these bits regardless of whether the port is configured as input or output.

Dedicated Digital Input (DI3-DI5) — The states of the three dedicated digital inputs are read from these bits.

Analog Multiplexer Address (A0-A3) — The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) — The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

3

ANALOG SUBSYSTEM
(See Block Diagram)

General Description

The analog subsystem of the MC14444 is composed of a 16-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of sixteen channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as V_{DD} and V_{SS} power supply rejection.

Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14444 allows 2 enable clock cycles for the write into the control register even if only 8 bits are written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 KΩ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte, and the interrupt request (IRQ) pin goes low if interrupt has been enabled by the IE bit of the control register. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logical 0) if an A/D conversion is in progress.

FIGURE 3 — TYPICAL A/D TIMING SEQUENCE

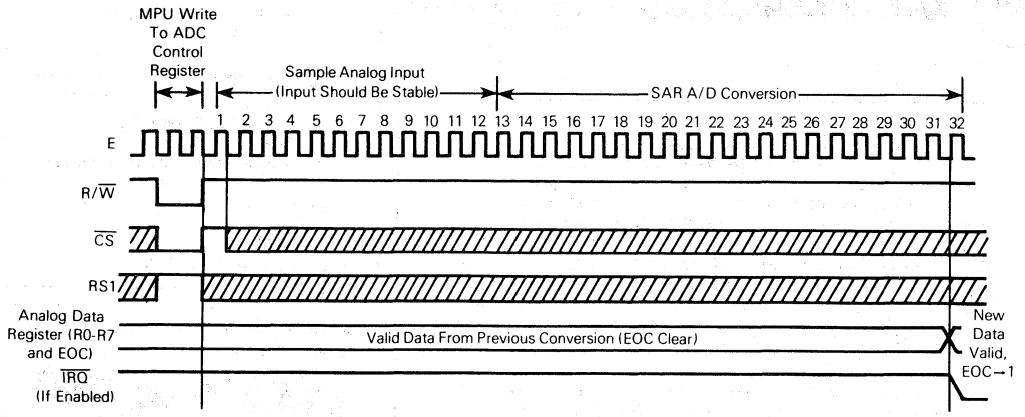
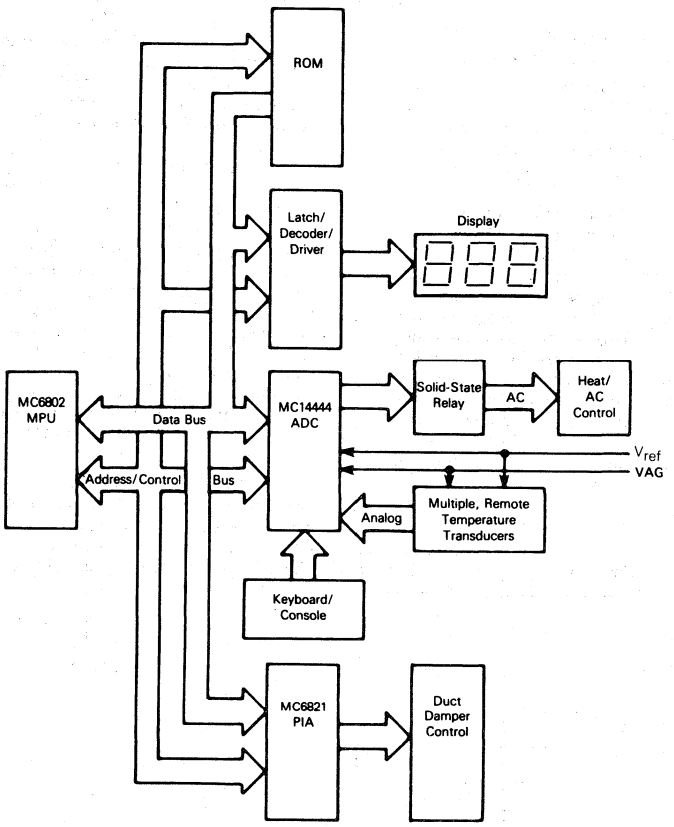


FIGURE 4 — TYPICAL MC14444 APPLICATION IN A CLIMATE CONTROLLER



MOTOROLA

MC14447

FOR COMPLETE DATA
SEE MC14443

ANALOG-TO-DIGITAL CONVERTER LINEAR SUBSYSTEM

The MC14443 and the MC14447 are 6-channel, single-slope, 8-10 bit analog-to-digital converter linear subsystems for microprocessor-based data and control systems. Contained in both devices are a one-of-8 decoder, an 8-channel analog multiplexer, a buffer amplifier, a precision voltage-to-current converter, a ramp start circuit, and a comparator. The output driver of the MC14443's comparator is an open-drain N-channel which provides a sinking current. The output driver of the MC14447's comparator is a standard B-Series P-Channel, N-Channel pair.

A CMOS MPU or MCU provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog-to-digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

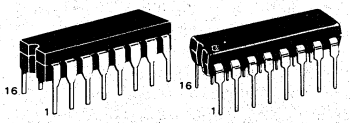
- Quiescent Current 0.8 mA Typical at V_{DD} = 5 V
- Single Supply Operation +4.5 to +18 Volts
- Direct Interface to CMOS MPUs
- Typical Resolution — 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} − 2 V
- Chip Complexity: MC14443 — 150 FETs
  MC14447 — 151 FETs

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

MICROPROCESSOR-BASED ANALOG-TO-DIGITAL CONVERTER

3



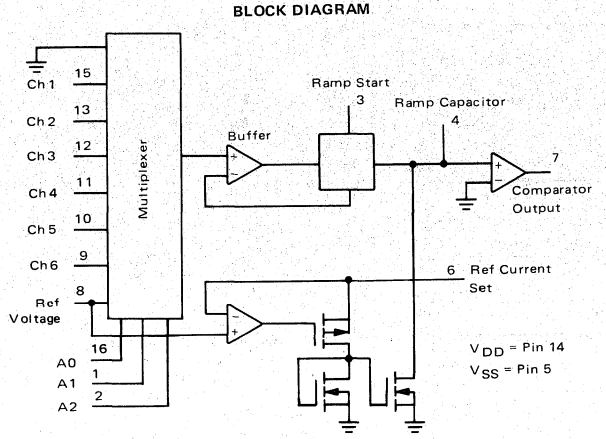
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

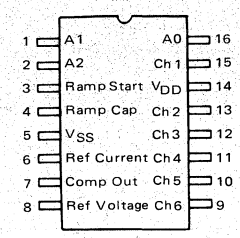
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT



MOTOROLA

MC14549B
MC14559B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

SUCCESSIVE APPROXIMATION REGISTERS

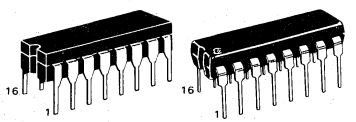
3

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when more than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog-to-digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 488 FETs or 122 Equivalent Gates



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
DC Input Current, per Pin	I_{in}	±10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TRUTH TABLES

MC14549B

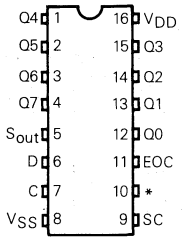
SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	↓	None
X	X	1	X	↑	Reset
1	0	0	0	↑	Start Conversion
1	X	0	1	↑	Start Conversion
1	1	0	0	↑	Continue Conversion
0	X	0	X	↑	Continue Previous Operation

MC14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	↓	None
1	0	0	↑	Start Conversion
X	1	0	↑	Continue Conversion
0	0	0	↑	Continue Conversion
0	X	1	↑	Retain Conversion Result
1	X	1	↑	Start Conversion

X = Don't Care
t-1 = State at Previous Clock ↑

PIN ASSIGNMENT



*For MC14549B Pin 10 is MR input
For MC14559B Pin 10 is FF input

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage#	"0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)		I_{OH}									mA
(V_{OH} = 2.5 V)	Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 V)			5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 V)			10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 V)			15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	1.28	–	1.02	1.76	–	0.72	–	mA
(V_{OL} = 0.5 V)	Q Outputs		10	3.2	–	2.6	4.5	–	1.8	–	
(V_{OL} = 1.5 V)			15	8.4	–	6.8	17.6	–	4.8	–	
(V_{OL} = 0.4 V)	Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 V)	Pin 5, 11 only		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mA
(V_{OH} = 2.5 V)	Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 V)			5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 V)			10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 V)			15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	1.04	–	0.88	1.76	–	0.72	–	mA
(V_{OL} = 0.5 V)	Q Outputs		10	2.6	–	2.2	4.5	–	1.8	–	
(V_{OL} = 1.5 V)			15	7.2	–	6.0	17.6	–	4.8	–	
(V_{OL} = 0.4 V)	Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)	Pin 5, 11 only		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μA
(Per Package)			10	–	10	–	0.010	10	–	300	
(Clock = 0 V,			15	–	20	–	0.015	20	–	600	
Other Inputs = V_{DD} or 0 V, I_{out} = 0 μA)											
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	20	–	0.005	20	–	150	μA
(Per Package)			10	–	40	–	0.010	40	–	300	
(Clock = 0 V,			15	–	80	–	0.015	80	–	600	
Other Inputs = V_{DD} or 0 V, I_{out} = 0 μA)											
Total Supply Current** †		I_T	5.0	I_T = (0.8 μA/kHz) f + I_{DD}							μA
(Dynamic plus Quiescent,			10	I_T = (1.6 μA/kHz) f + I_{DD}							
Per Package)			15	I_T = (2.4 μA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all											
buffers switching)											

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

\# Noise immunity specified for worst-case input combination
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

† To calculate total supply current at loads other than 50 pF
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3}(C_L - 50)\ V_{DD} f$
where I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency

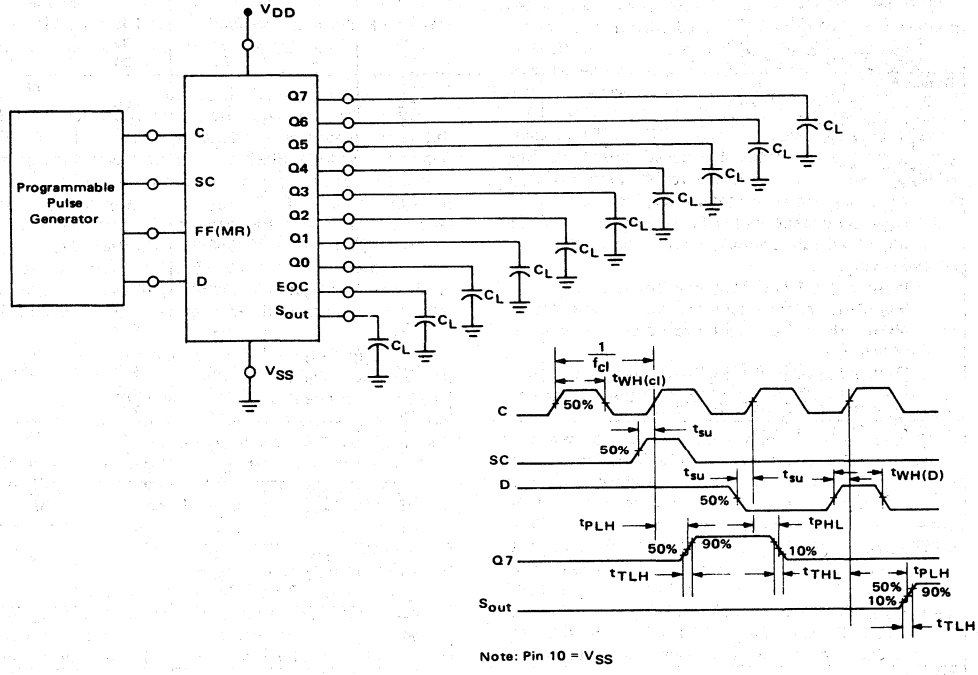
** The formulas given are for the typical characteristics only at 25°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	420	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	310	
Clock to S_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 277 ns		10	–	310	620	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	440	
Clock to EOC						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/ pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
SC, D, FF or MR Setup Time	t_{su}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Clock Pulse Width	$t_{WH(cl)}$	5.0	700	350	–	ns
		10	270	135	–	
		15	200	100	–	
Pulse Width – D, SC, FF or MR	t_{WH}	5.0	500	250	–	ns
		10	200	100	–	
		15	160	80	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Clock Pulse Frequency	f_{cl}	5.0	–	1.5	0.8	MHz
		10	–	3.0	1.5	
		15	–	4.0	2.0	

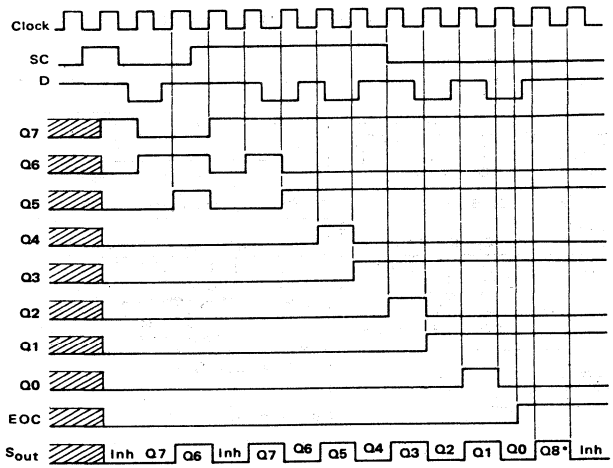
* The formulae given are for the typical characteristics only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Pin 10 = V_{SS}

TIMING DIAGRAM



– Don't care condition

Inh – Indicates Serial Out is inhibited low.

* – Q8 is ninth-bit of serial information available from 8-bit register.

Note: Pin 10 = V_{SS}

OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock – A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert – A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

D = Data In – Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B only) – Resets all output to 0 on positive-going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B only) – Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded.

For 8-bit operation, FF is tied to V_{SS}.

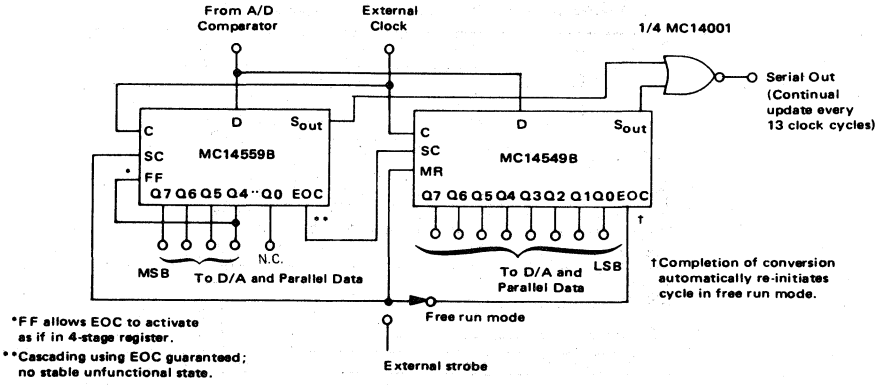
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (S_{out}) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while S_{out} of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs – After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert – This output goes high on the negative-going transition of the clock following FF = 1 (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out – Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 – 12-BIT CONVERSION SCHEME



TYPICAL APPLICATIONS

Externally Controlled 6-Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8-Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12-Bit ADC (Figure 4)

Because each successive approxiamtion register (SAR) has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch-on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non-functional condition.

This 12-bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of

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FIGURE 2 – EXTERNALLY CONTROLLED 6-BIT ADC

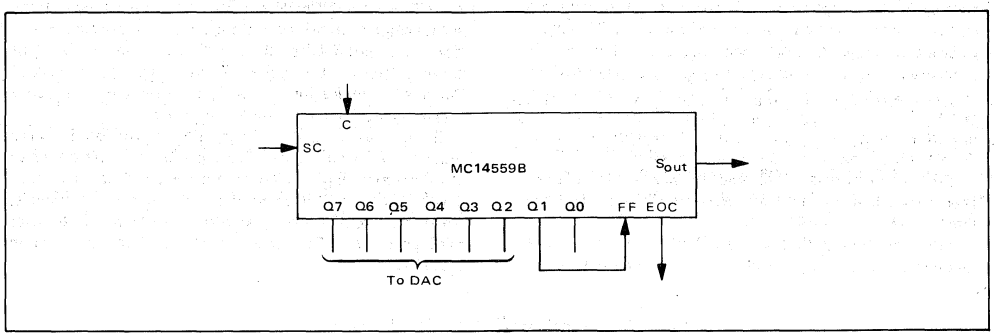


FIGURE 3 – CONTINUOUSLY CYCLING 8-BIT ADC

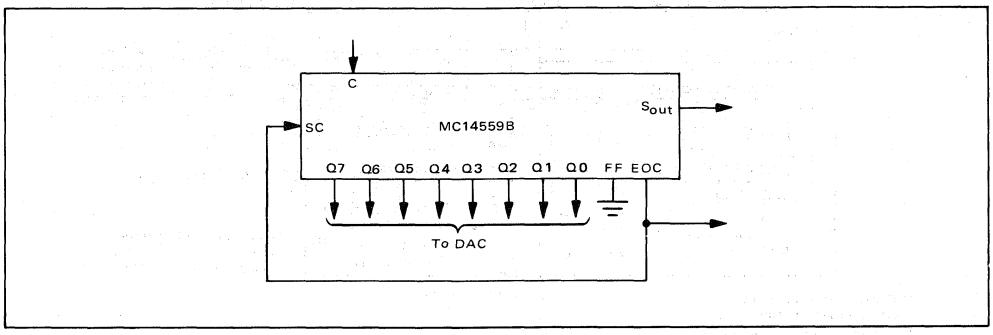
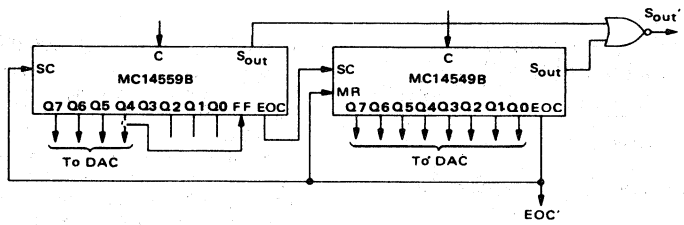


FIGURE 4 – CONTINUOUSLY CYCLING 12-BIT ADC



the 12-bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

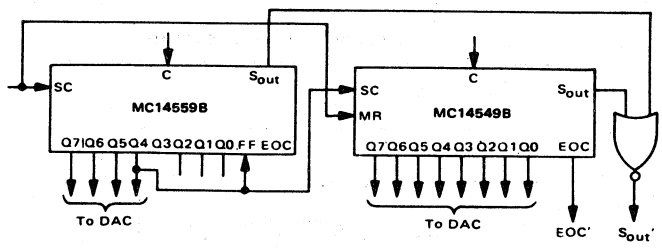
Additional Motorola Parts for Successive Approximation ADC

Monolithic digital-to-analog converters – The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** – The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

FIGURE 5 – EXTERNALLY CONTROLLED 12-BIT ADC



MOTOROLA

MC144110
MC144111

Advance Information

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

DIGITAL-TO-ANALOG CONVERTERS WITH SERIAL INTERFACE

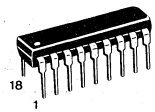
3

DIGITAL-TO-ANALOG CONVERTERS WITH SERIAL INTERFACE

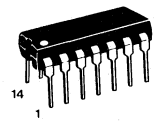
The MC144110 and MC144111 are low-cost six-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 volt supply range, they may be directly interfaced to CMOS MPUs operating at 5 volts.

- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS μP
- Wide Operating Voltage Range: 4.5 to 15 Volts
- Wide Operating Temperature Range: 0 to 85°C

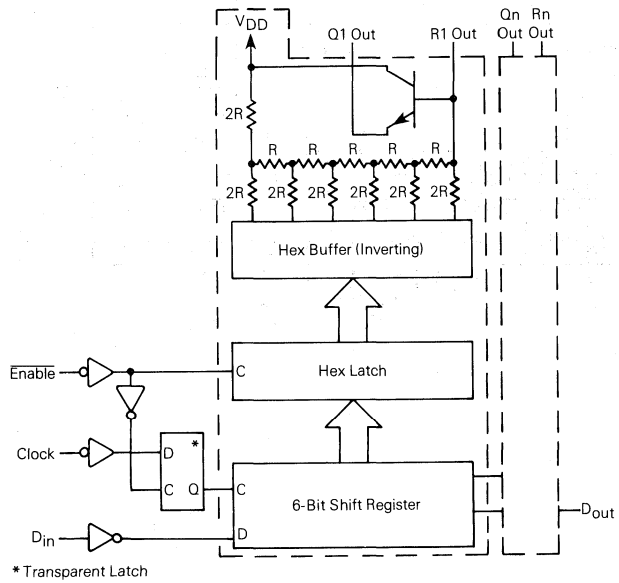


MC144110
P SUFFIX
PLASTIC PACKAGE
CASE 707



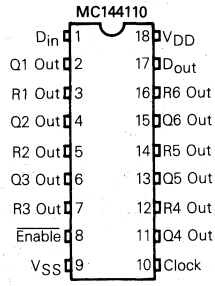
MC144111
P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM

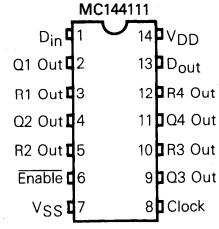


PIN ASSIGNMENTS

MC144110



MC144111



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I	±10	mA
Power Dissipation (Per Output) T_A=70°C, MC144110 MC144111 T_A=85°C, MC144110 MC144111	P_{OH}	 30 50 10 20	mW
Power Dissipation (Per Package) T_A=70°C, MC144110 MC144111 T_A=85°C, MC144110 MC144111	P_D	 100 150 25 50	mW
Storage Temperature Range	T_{stg}	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

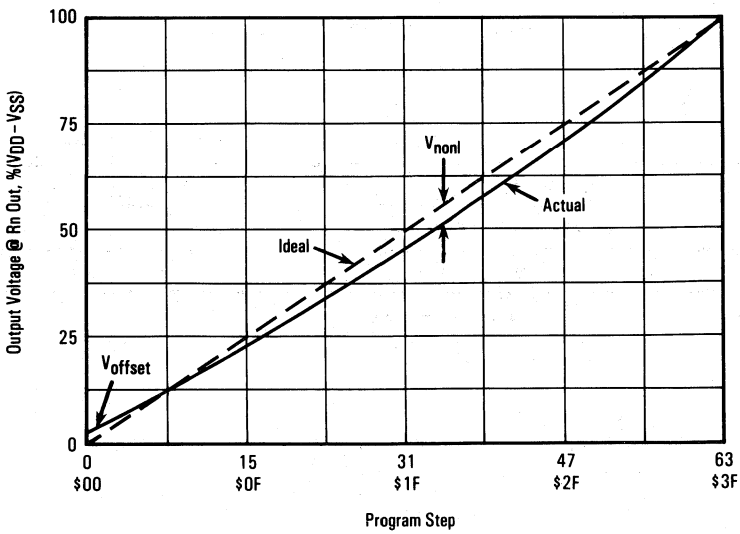
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=0° to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High-Level Input Voltage (D_{in}, $\overline{Enable}$, Clock)		5 10 15	3.0 3.5 4.0	– – –	V
V_{IL}	Low-Level Input Voltage (D_{in}, $\overline{Enable}$, Clock)		5 10 15	– – –	0.8 0.8 0.8	V
I_{OH}	High-Level Output Current (D_{out})	$V_{out}=V_{DD}-0.5$ V	5 10 15	−200	– – –	μA
I_{OL}	Low-Level Output Current (D_{out})	V_{out}=0.5 V	5 10 15	200	– – –	μA
I_{DD}	Quiescent Supply Current	I_{out}=0 μA MC144110 MC144111	15 15	– –	12 8	mA
I_{in}	Input Leakage Current (D_{in}, $\overline{Enable}$, Clock)	$V_{in}=V_{DD}$ or 0 V	15	–	±1	μA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 1	5 10 15	– – –	100 200 300	mV
V_{step}	Step Size (Rn Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
V_{offset}	Offset Voltage from V_{SS}	D_{in}=$00, See Figure 1	–	–	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$=0 V	15	–	10	μA
h_{FE}	DC Current Gain	I_E=0.1 to 10.0 mA T_A=25°C	–	40	–	–
V_{BE}	Base-to-Emitter Voltage Drop	I_E=1.0 mA	–	0.4	0.7	V

SWITCHING CHARACTERISTICS (Voltages Referenced to V_{SS}, $T_A = 0$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 20$ ns Unless Otherwise Indicated)

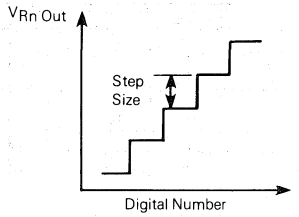
Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pulse Width, Clock (Figures 3 and 4)	5 10 15	2 1.5 1	– – –	μs
t_{wL}	Negative Pulse Width, Clock (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	μs
t_{su}	Setup Time, $\overline{Enable}$ to Clock (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	μs
t_{su}	Setup Time, D_{in} to Clock (Figures 3 and 4)	5 10 15	1000 750 500	– – –	ns
t_h	Hold Time, Clock to $\overline{Enable}$ (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	μs
t_h	Hold Time, Clock to D_{in} (Figures 3 and 4)	5 10 15	5 3.5 2	– – –	μs
t_{PLH}, t_{PHL}	Propagation Delay, Clock to D_{out}	5 10 15	– – –		ns
t_r, t_f	Input Rise and Fall Times	5-15	–	2	μs
t_{TLH}, t_{THL}	Output Transition Time, D_{out}	5 10 15	– – –		ns
C_{in}	Input Capacitance	5-15	–	7.5	pF

FIGURE 1 — D/A TRANSFER FUNCTION



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of linearity of the actual transfer function from the best-fit straight line. It is normally specified in parts of an LSB.

FIGURE 2 — DEFINITION OF STEP SIZE



$$\text{Step size} = \frac{V_{DD}}{64} \pm 0.75\frac{V_{DD}}{64}$$

(For any adjacent pair of digital numbers)

FIGURE 3 — SERIAL INPUT, POSITIVE CLOCK

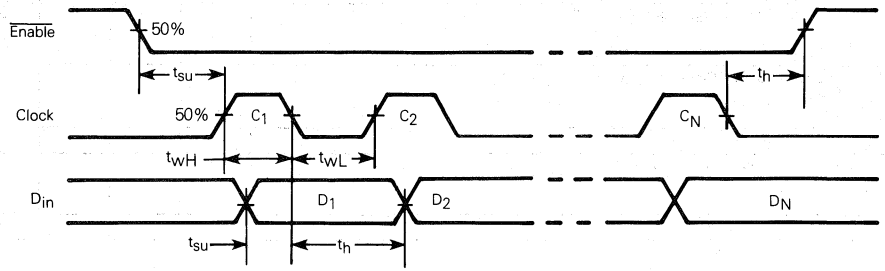
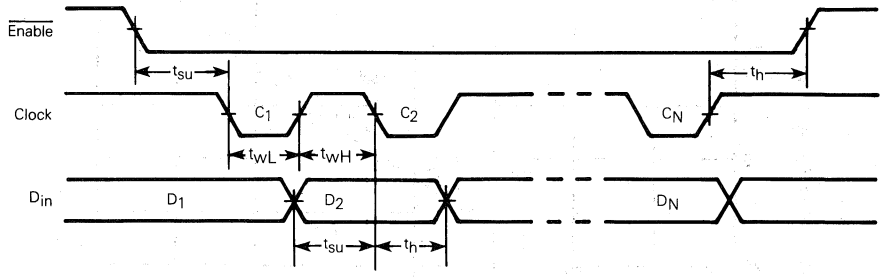


FIGURE 4 — SERIAL INPUT, NEGATIVE CLOCK



PIN DESCRIPTIONS

INPUTS

D_{in}, DATA INPUT – Six-bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

$\overline{\text{Enable}}$, NEGATIVE LOGIC ENABLE – The $\overline{\text{Enable}}$ pin must be low (active) during the serial load. On the low-to-high transition of $\overline{\text{Enable}}$, data contained in the shift register is loaded into the latch.

Clock, SHIFT REGISTER CLOCK – Data is shifted into the register on the high-to-low transition of Clock. Clock is fed into the D-input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{\text{Enable}}$ is high.

OUTPUTS

D_{out}, DATA OUTPUT – The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out, RESISTOR NETWORK OUTPUTS – These are the R-2R resistor network outputs. These outputs may be fed to high-impedance input FET op amps to bypass the on-chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out, NPN TRANSISTOR OUTPUTS – Buffered DAC outputs utilize an emiter-follower configuration for current-gain, thereby allowing interface to low-impedance circuits.

SUPPLY PINS

V_{SS}, NEGATIVE SUPPLY VOLTAGE – This pin is usually ground.

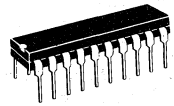
V_{DD}, POSITIVE SUPPLY VOLTAGE – The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 volts, peak-to-peak.

MOTOROLA

Advance Information

8-Bit A/D Converters With Serial Interface

Silicon-Gate CMOS



CERAMIC CASE 732 PLASTIC CASE 738

PLASTIC LEADED CHIP CARRIER (PLCC) CASE 775

ORDERING INFORMATION

MC14XXXX

Suffix
- 1 2.5 V ≤ V_{ref} ≤ V_{DD}
- 2 $V_{ref} = V_{DD}$
- P Plastic (−40 to +85°C)
- L Ceramic (−55 to +125°C)
- FN PLCC (−40 to +85°C)

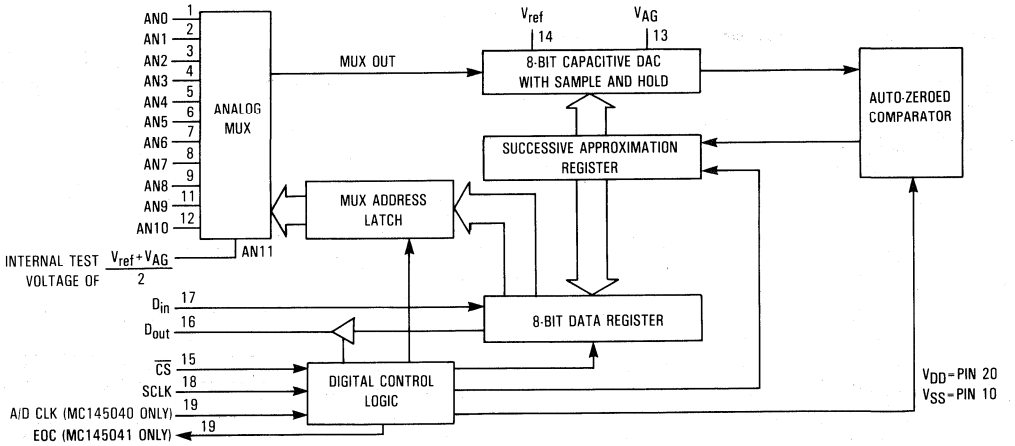
3

The MC145040 and MC145041 are low-cost 8-bit A/D Converters with serial interface ports to provide communication with microprocessors and microcomputers. The converters operate from a single power supply with a maximum nonlinearity of ± ½ LSB over the full temperature range. No external trimming is required.

The MC145040 allows an external clock input (A/D CLK) to operate the dynamic A/D conversion sequence. The MC145041 has an internal clock and an end-of-conversion signal (EOC) is provided.

- Operating Voltage Range: V_{DD} = 4.5 to 5.5 Volts
- Successive Approximation Conversion Time:
  - MC145040 — 10 μs (with 2 MHz A/D CLK)
  - MC145041 — 20 μs Maximum (Internal Clock)
- 11 Analog Input Channels with Internal Sample and Hold
- 0- to 5-Volt Analog Input Range with Single 5-Volt Supply
- Ratiometric Conversion
- Separate V_{ref} and V_{AG} Pins for Noise Immunity
- Monotonic Over Voltage and Temperature
- No External Trimming Required
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- TTL/NMOS-Compatible Inputs May Be Driven with CMOS
- Outputs are CMOS, NMOS, or TTL Compatible
- Very Low Reference Current Requirement
- Low Power Consumption: 11 mW
- Internal Test Mode for Self Test

BLOCK DIAGRAM



MICROWIRE is a trademark of National Semiconductor.

This document contains information on a new product. Specification and information herein are subject to change without notice.

MAXIMUM RATINGS* (For all product grades)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +7.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} − 0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS} − 1.5 to V_{DD} + 1.5	V
V_{out}	DC Output Voltage	V_{SS} − 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD},I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.) Unused outputs must be left open.

3

OPERATION RANGES (Applicable to Guaranteed Limits for all product grades)

Symbol	Parameter	Suffix				Unit
		L1	L2	P1, FN1	P2, FN2	
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V
V_{ref}	DC Reference Voltage (Note 1)	V_{AG} + 2.5 to V_{DD}	V_{DD}	V_{AG} + 2.5 to V_{DD}	V_{DD}	V
V_{AG}	Analog Ground (Note 1)	V_{SS} to V_{ref} − 2.5	V_{SS}	V_{SS} to V_{ref} − 2.5	V_{SS}	V
V_{AI}	Analog Input Voltage (Note 2)	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
T_A	Operating Temperature	−55 to +125	−55 to +125	−40 to +85	−40 to +85	°C

NOTES:
1. Reference voltages down to 1.0 V ($V_{ref} - V_{AG} = 1.0$ V) are functional, but the A/D Converter Electrical Characteristics are not guaranteed.
2. $V_{SS} \le V_{AI} \le V_{AG}$ produces an output of $00 and $V_{ref} \le V_{AI} \le V_{DD}$ produces an output of $FF. See V_{AG} and V_{ref} pin descriptions.

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Symbol	Parameter	Test Conditions	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	I_{out} = −200 μA I_{out} = −100 μA I_{out} = −20 μA	2.4 2.4 V_{DD} − 0.1	V
V_{OL}	Maximum Low-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	I_{out} = +1.6 mA I_{out} = +1.0 mA I_{out} = 20 μA	0.4 0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, A/D CLK)	$V_{in} = V_{SS}$ or V_{DD}	±2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	$V_{out} = V_{SS}$ or V_{DD}	±10	μA
I_{DD}	Maximum Power Supply Current	$V_{in} = V_{SS}$ or V_{DD}, All Outputs Open MC145040: A/D CLK = 2 MHz	2	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	$V_{ref} = V_{DD}$ $V_{AG} = V_{SS}$	10	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input. (AN0-AN10)	$V_{AI} = V_{SS}$ to V_{DD}, L1 and L2 Suffix P1,P2, FN1, FN2 Suffix	±1000 ±400	nA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(MC145040: 1 MHz ≤ A/D CLK ≤ 2 MHz, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Minimum Resolution	Number of bits resolved by the A/D	8	Bits
Maximum Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	± ½	LSB
Maximum Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	± ½	LSB
Maximum Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	± ½	LSB
Maximum Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	± ½	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	±1	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion MC145040 MC145041	20 20	A/D CLK cycles μs
Maximum Data Transfer Time	Total time to transfer digital serial data into and out of the device	8	SCLK cycles
Maximum Sample Acquisition Time	Analog input acquisition time window MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz MC140541: SCLK = 1 MHz	 10 16	μs
Maximum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz MC145041: SCLK = 1 MHz	 24 40	μs
Maximum Sample Rate	Rate at Which Analog Inputs May be Sampled MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz MC145041: SCLK = 1 MHz	 41 25	kHz

AC ELECTRICAL CHARACTERISTICS ($t_r = t_f = 6$ ns, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Figure	Symbol	Parameter	Guaranteed Limit	Unit
1	f	Maximum Clock Frequency (50% Duty Cycle), SCLK	1.1	MHz
1 (same as SCLK)	f	Clock Frequency (50% Duty Cycle), A/D CLK (MC145040) Minimum Maximum	1.0 2.1	MHz
1,7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}	400	ns
1,7	t_h	Minimum Hold Time, SCLK to D_{out}	10	ns
2,7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}	150	ns
2,7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out} MC145040 MC145041	3 A/D CLK cycles + 400 ns 3.4 μs	
3	t_{su}	Minimum Setup Time, D_{in} to SCLK	400	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}	0	ns
4,7,8	t_d	Maximum Delay Time, EOC to D_{out} (MSB) MC145041	400	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK MC145040 MC145041	3 A/D CLK cycles + 800 ns 3.8 μs	
5	t_h	Minimum Hold Time, 8th SCLK to $\overline{CS}$	0	ns
6,8	t_{PHL}	Maximum Propagation Delay, 8th SCLK to EOC	500	ns
1	t_r, t_f	Maximum Input Rise and Fall Times, Any Digital Input	100	ns
1,4,6,7,8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	300	ns
—	C_{in}	Maximum Input Capacitance AN0-AN10 A/D CLK, SCLK, $\overline{CS}$, D_{in}	55 15	pF
—	C_{out}	Maximum Three-State Output Capacitance D_{out}	15	pF

SWITCHING WAVEFORMS

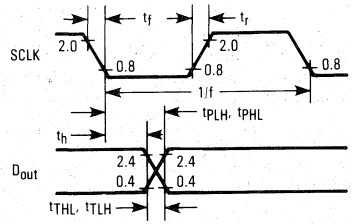


Figure 1

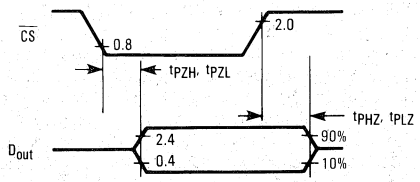


Figure 2

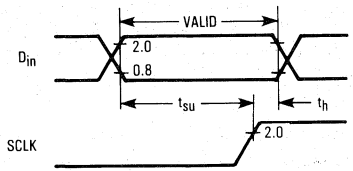


Figure 3

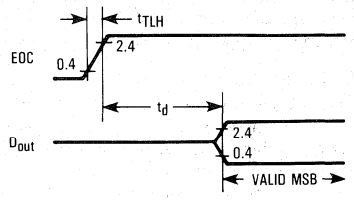


Figure 4

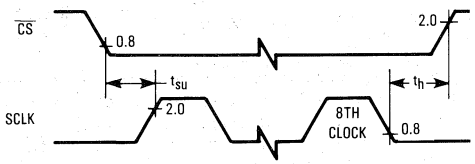


Figure 5

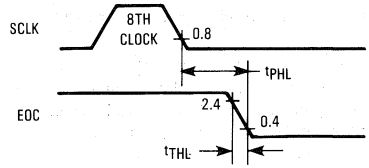


Figure 6

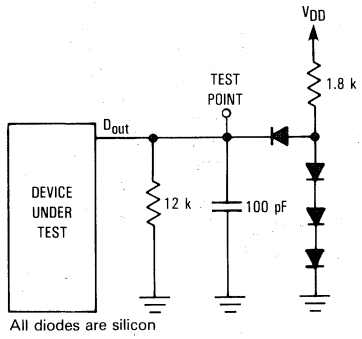


Figure 7. Test Circuit

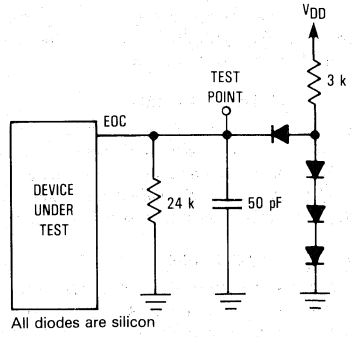


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUTS

$\overline{CS}$ (Pin 15)

Active-low chip select input. $\overline{CS}$ provides three-state control of D_{out}. $\overline{CS}$ at a high logic level forces D_{out} to a high-impedance state. In addition, the device recognizes the falling edge of $\overline{CS}$ as a serial interface reset to provide synchronization between the MPU and the A/D converter's serial data stream. To prevent a spurious reset from occurring due to noise on the $\overline{CS}$ input, a delay circuit has been included such that a $\overline{CS}$ signal of duration $\leq$1 A/D CLK period (MC145040) or $\leq$500 ns (MC145041) is ignored. A valid $\overline{CS}$ signal is acknowledged when the duration is $\geq$3 A/D CLK periods (MC145040) or $\geq 3\ \mu s$ (MC145041).

CAUTION

A reset aborts a conversion sequence, therefore high-to-low transitions on $\overline{CS}$ must be avoided during the conversion sequence.

D_{out} (Pin 16)

Serial data output of the A/D conversion result. The 8-bit serial data stream begins with the most significant bit and is shifted out on the high-to-low transition of SCLK. D_{out} is a three-state output as controlled by $\overline{CS}$. However, D_{out} is forced into a high-impedance state after the eighth SCLK, independent of the state of $\overline{CS}$. See Figures 9, 10, 11, or 12.

D_{in} (Pin 17)

Serial data input. The 4-bit serial data stream begins with the most significant address bit of the analog mux and is shifted in on the low-to-high transition of SCLK.

SCLK (Pin 18)

Serial data clock. The serial data register is completely static, allowing SCLK rates down to DC in a continuous or intermittent mode. SCLK need not be synchronous to the A/D CLK (MC145040) or the internal clock (MC145041). Eight SCLK cycles are required for each simultaneous data transfer, the low-to-high transition shifting in the new address and the high-to-low transition shifting out the previous conversion result. The address is acquired during the first four SCLK cycles, with the interval produced by the remaining four cycles being used to begin charging the on-chip sample-and-hold capacitors. After the eighth SCLK, the SCLK input is inhibited (on-chip) until the conversion is complete.

A/D CLK (Pin 19, MC145040 only)

A/D clock input. This pin clocks the dynamic A/D conversion sequence, and may be asynchronous and unrelated to SCLK. This signal must be free running, and may be obtained from the MPU system clock. Deviations from a 50% duty cycle can be tolerated if each half period is > 238 ns.

EOC (Pin 19, MC145041 only)

End-of-conversion output. EOC goes low on the negative edge of the eighth SCLK. The low-to-high transition of EOC indicates the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10 (Pins 1-9, 11, 12)

Analog multiplexer inputs. The input AN0 is addressed by loading $0 into the serial data input, D_{in}. AN1 is addressed by $1, AN2 by $2 . . . AN10 via $A. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source impedance driving these inputs must be $\leq$10 kΩ. NOTE: $B addresses an on-chip test voltage of $(V_{ref} + V_{AG})/2$, and produces an output of $80 if the converter is functioning properly. However, a $\pm$1 LSB deviation from $80 occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD} (Pins 10 and 20)

Device supply pins. V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. $V_{DD} - V_{SS}$ variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets > ½ LSB.

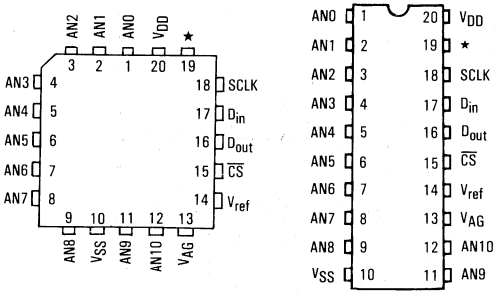
V_{AG} and V_{ref} (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages $\geq V_{ref}$ produce an output of $FF and input voltages $\leq V_{AG}$ produce an output of $00. CAUTION: The analog input voltage must be $\geq V_{SS}$ and $\leq V_{DD}$. The A/D conversion result is ratiometric to $V_{ref} - V_{AG}$ as shown by the formula:

$$V_{in} = \left[\frac{\text{output code}}{\$FF} \times (V_{ref} - V_{AG})\right] + \frac{\text{quantizing}}{\text{error}} + \frac{\text{linearity}}{\text{error}}$$

V_{ref} and V_{AG} should be as noise-free as possible to avoid degradation of the A/D conversion. Noise on either of these pins will couple 1:1 to the analog input signal, i.e. a 20 mV change in V_{ref} can cause a 20 mV error in the conversion result. Ideally V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers.

PIN ASSIGNMENTS



★NOTE:
A/D CLK (MC145040)
EOC (MC145041)

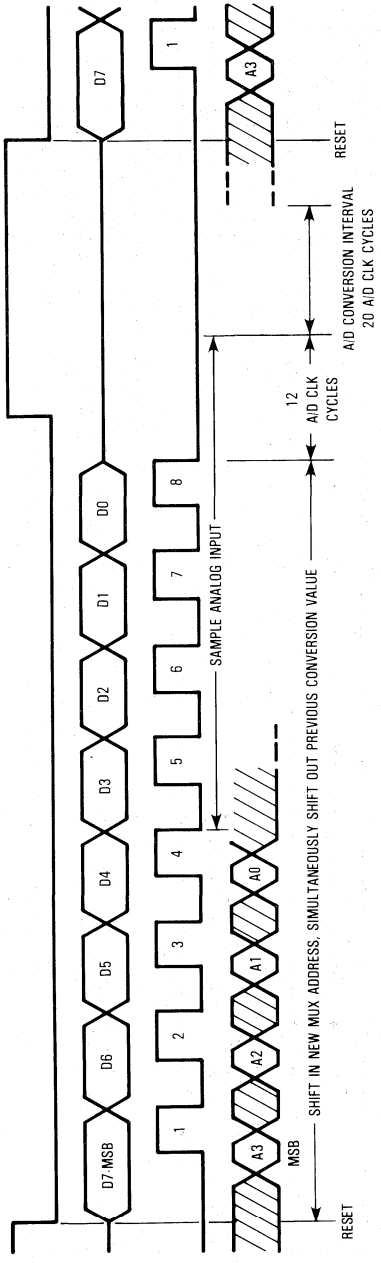


Figure 9. MC145040 Timing Diagram Utilizing $\overline{CS}$ to Three-State D_{out}

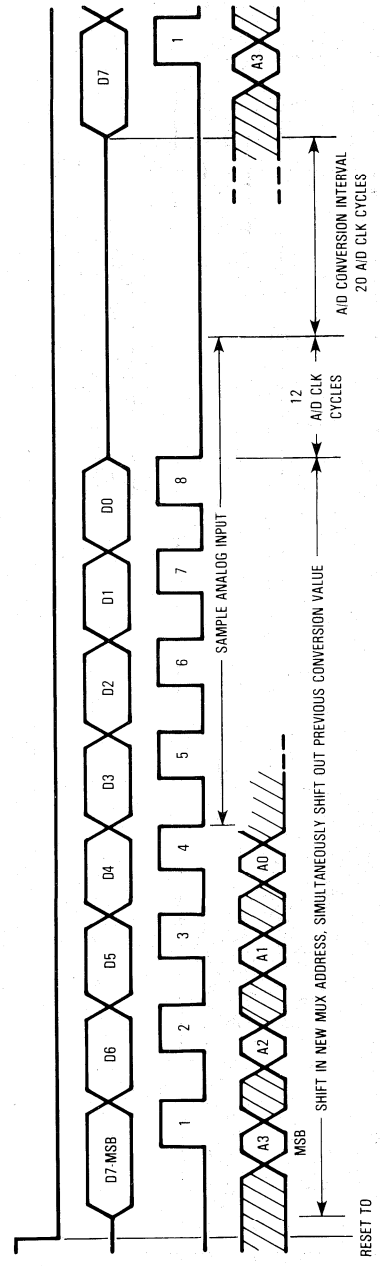


Figure 10. MC145040 Timing Diagram Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

3

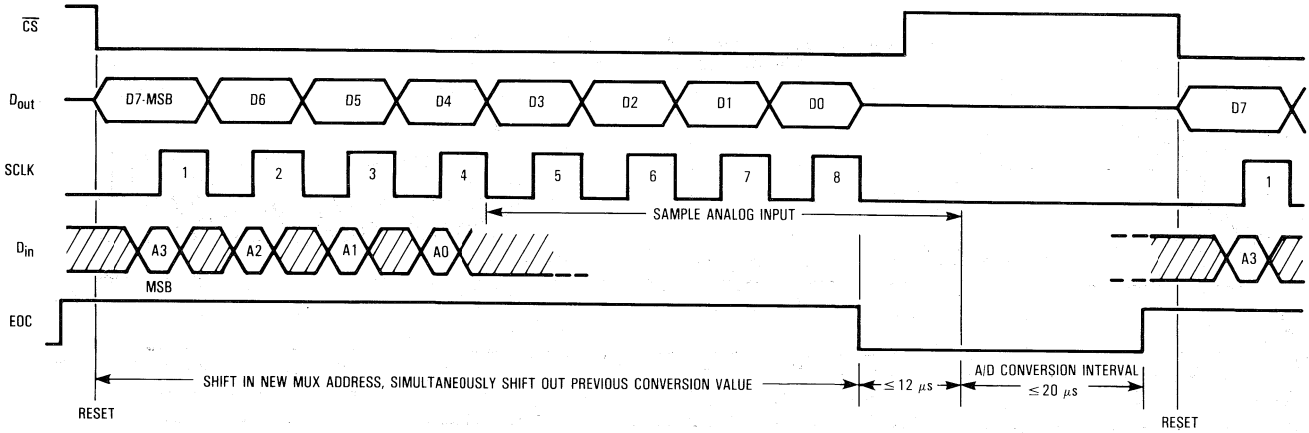


Figure 11. MC145041 Timing Diagram
Utilizing $\overline{CS}$ to Three-State D_{out}

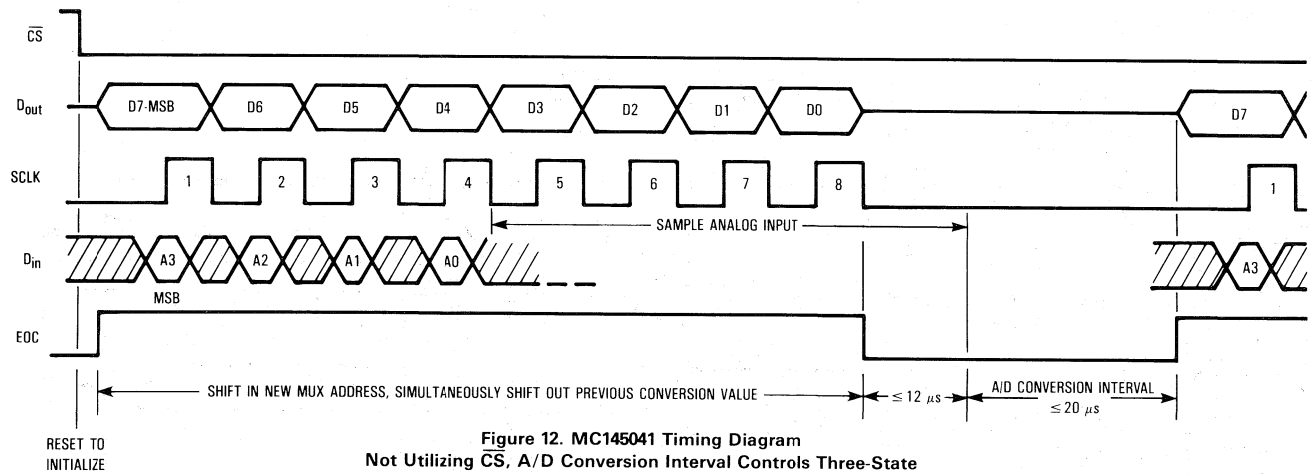


Figure 12. MC145041 Timing Diagram
Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

APPLICATIONS INFORMATION

DESCRIPTION

This example application of the MC145040/MC145041 ADCs interfaces three controllers to a microprocessor and processes data in real-time for a video game. The standard joystick X-axis (left/right) and Y-axis (up/down) controls as well as engine thrust controls are accommodated.

Figure 13 illustrates how the MC145040/MC145041 is used as a cost-effective means to simplify this type of circuit design. Utilizing one ADC, three controllers are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SPI) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs may be used if power consumption is not critical. A V_{DD} to V_{SS} 0.1 μF bypass capacitor should be closely mounted to the ADC.

Both the MC145040 and MC145041 will accommodate all the analog system inputs. The MC145040, when used with a 2 MHz MCU, takes 24 μs to sample the analog input, perform the conversion, and transfer the serial data at 1 MHz. Thirty-two A/D Clock cycles (2 MHz at input pin 19) must be provided and counted by the MCU after the eighth SCLK before reading the ADC results. The MC145041 has the end-of-conversion (EOC) signal (at output pin 19) to define when data is ready, but has a slower 40 μs cycle time. However, the 40 μs is constant for serial data rates of 1 MHz independent of the MCU clock frequency. Therefore, the MC145041 may be used with the CMOS MCU operating at reduced clock rates to minimize power consumption without sacrificing ADC cycle times, with EOC being used to generate an interrupt. (The MC145041 may also be used with MCUs which do not provide a system clock.)

ANALOG DESIGN CONSIDERATIONS

Controllers with output impedances of less than 10 kilohms may be directly interfaced to these ADCs, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 13, the V_{ref} and controller output lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil-shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair or the shield must be V_{AG}.

A reference circuit voltage of 5 volts is used for this application. The reference circuitry may be as simple as tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 14.) However, the system power supply noise may require that a separate supply be used for the voltage reference. This supply must provide source current for V_{ref} as well as current for the controller potentiometers.

A bypass capacitor across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straightforward. The nine analog inputs, AN0 through AN8, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to be read to the ADC, simultaneously. All nine inputs may be scanned in a minimum of 216 μs (MC145040) or 360 μs (MC145041).

If the design is realized using the MC145040, 32 A/D clock cycles (at pin 19) must be counted by the MCU to allow time for A/D conversion. The designer utilizing the MC145041 has the end-of-conversion signal (at pin 19) to define the conversion interval. EOC may be used to generate an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data, and transfer the information to the video circuitry for updating the display.

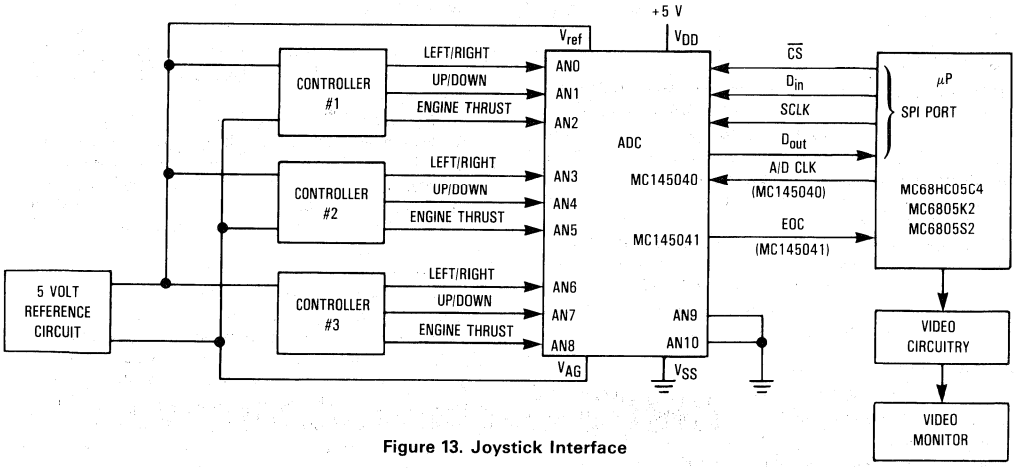


Figure 13. Joystick Interface

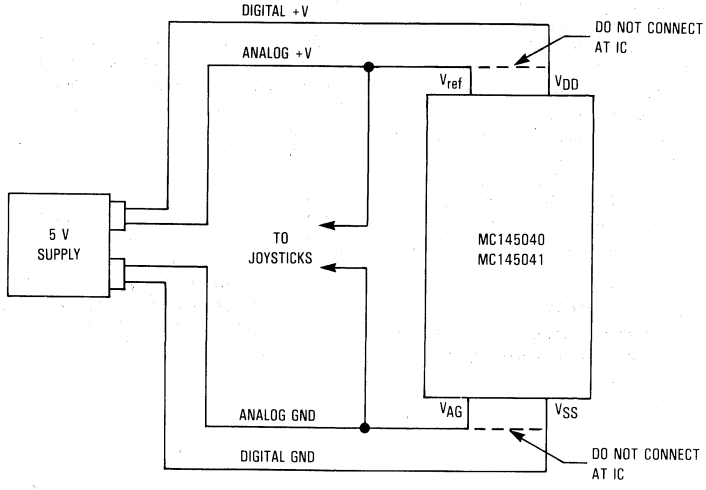


Figure 14. Alternate Configuration Using the Digital Supply for the Reference Voltage

CMOS Decoders/Display Drivers

4

CMOS DECODERS/DISPLAY DRIVERS

Device Number	Function
MC14495-1	Hexadecimal-to-7-Segment Latch/Decoder ROM/Driver
MC14499	7-Segment LED Display Decoder/Driver with Serial Interface
MC14511B	BCD-to-7-Segment Latch/Decoder/Driver
MC14513B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking
MC14547B	High-Current BCD-to-7-Segment Decoder/Driver
MC14558B	BCD-to-7-Segment Decoder
MC145000	Serial Input Multiplexed LCD Driver (Master)
MC145001	Serial Input Multiplexed LCD Driver (Slave)
MC145453	LCD Driver with Serial Interface

4

Display Type	Input Format	Drive Capability Per Package	On-Chip Latch	Display Control Inputs	Segment Drive Current	Device Number	Number of Pins
LCD	Parallel BCD	7 Segments	✓	Blank	~1 mA	MC14543B	16
			✓	Blank, Ripple Blank	~1 mA	MC14544B	18
	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	33 Segments or Dots	✓		20 μA	MC145453	40
Muxed LCD	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	48 Segments or Dots	✓		~200 μA	MC145000	24
		44 Segments or Dots	✓		~200 μA	MC145001	18
LED, Incandescent, Fluorescent*	Parallel BCD	7 Segments	✓	Blank, Lamp Test	25 mA	MC14511B	16
			✓	Blank, Ripple Blank, Lamp Test	25 mA	MC14513B	18
				Blank	65 mA	MC14547B	16
LED, Incandescent	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	28 Segments + 4 Decimal Points	✓	Oscillator (Scanner)	50 mA	MC14499	18
LED	Parallel Hex	7 Segments + A thru F Indicator	✓		10 mA★	MC14495-1	16
(Interfaces to Display Drivers)	Parallel BCD	7 Segments		Ripple Blank, Enable		MC14558B	16

*Absolute maximum working voltage = 18 V
★On-chip current-limiting resistor

MOTOROLA

MC14495-1

Advance Information

HEXADECIMAL-TO-SEVEN SEGMENT LATCH/ DECODER ROM/DRIVER

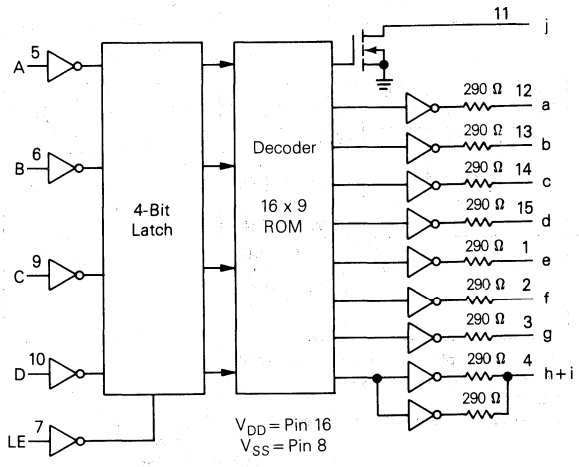
The MC14495-1 is constructed with CMOS enhancement-mode devices and NPN bipolar output drivers in a monolithic structure. The circuit provides the functions of a 4-bit storage latch. The decoder is implemented utilizing a mask-programmable ROM. With a 5-volt power supply, it can be used without resistor interface to drive seven segment LEDs. The series output resistors of, typically, 290 ohms are internal to the device.

The MC14495-1 is an improved version of the MC14495 with CMOS input levels and decreased propagation delays.

Applications include MPU systems display driver, instrument display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic-Circuit Power Dissipation
- High Current-Sourcing Outputs with Internal Limiting Resistors
- Latch Storage of Code
- Supply Voltage Range = 4.5 to 18 V
- CMOS Input Switching Levels
- Standard ROM Provides Hex-to-Seven Segment Decoding
- Other ROM Options Available Upon Request (Contact your Motorola Sales Office)
- Chip Complexity: 187 FETs plus 9 NPNs or 49 Equivalent Gates

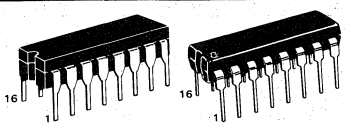
BLOCK DIAGRAM



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HEXADECIMAL-TO-SEVEN SEGMENT LATCH/DECODER ROM/DRIVER

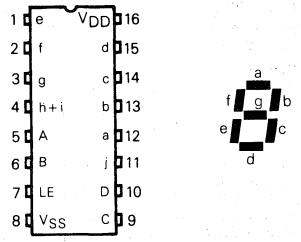


L SUFFIX
CERAMIC PACKAGE
CASE 620

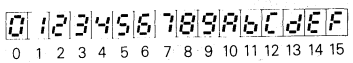
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L1 Ceramic Package
- P1 Plastic Package



ALPHANUMERIC DISPLAY



TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	a	b	c	d	e	f	g	h+i	j	DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	Open	0
0	0	0	1	0	1	1	0	0	0	0	0	Open	1
0	0	1	0	1	1	0	1	1	0	1	0	Open	2
0	0	1	1	1	1	1	1	0	0	1	0	Open	3
0	1	0	0	0	1	1	0	0	1	1	0	Open	4
0	1	0	1	1	0	1	1	0	1	1	0	Open	5
0	1	1	0	1	0	1	1	1	1	1	0	Open	6
0	1	1	1	1	1	1	0	0	0	0	0	Open	7
1	0	0	0	1	1	1	1	1	1	1	0	Open	8
1	0	0	1	1	1	1	1	0	1	1	0	Open	9
1	0	1	0	1	1	1	0	1	1	1	1	Open	A
1	0	1	1	0	0	1	1	1	1	1	1	Open	b
1	1	0	0	1	0	0	1	1	1	0	1	Open	C
1	1	0	1	0	1	1	1	1	0	1	1	Open	d
1	1	1	0	1	0	0	1	1	1	1	1	Open	E
1	1	1	1	1	0	0	0	1	1	1	1	0	F

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25°C Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	P_{OHmax}‡	 50 100	mW

‡ $P_{OHmax} = I_{OH}(V_{DD}-V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

4

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Input Voltage # "0" Level	V_{IL}									V
(V_O = 3.8 or 0.5 V)		5	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 V)		15	–	4.0	–	6.00	4.0	–	4.0	
(V_O = 0.5 or 3.8 V) "1" Level	V_{IH}	5	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 8.8 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage: a−g, h+i	V_{OL}	5	–	0.1	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0, $I_{out} = 0$ μA		10	–	0.1	–	0	0.05	–	0.05	
		15	–	0.1	–	0	0.05	–	0.05	
Output Drive Voltage: a−g, h+i	V_{OH}	5								V
(I_{OH} = 0 mA)			4.0	–	4.0	4.8	–	4.0	–	
(I_{OH} = 5 mA)			2.45	–	2.4	3.0	–	2.05	–	
(I_{OH} = 10 mA)			1.3	–	0.8	1.7	–	–	–	
(I_{OH} = 0 mA)		10	9.0	–	9.0	9.8	–	9.0	–	V
(I_{OH} = 5 mA)			7.4	–	7.2	8.0	–	6.9	–	
(I_{OH} = 10 mA)			6.4	–	5.8	6.7	–	5.0	–	
(I_{OH} = 15 mA)			5.3	–	4.4	5.3	–	3.05	–	
(I_{OH} = 0 mA)		15	14.0	–	14.0	14.8	–	14.0	–	V
(I_{OH} = 5 mA)			12.2	–	12.0	13.0	–	11.7	–	
(I_{OH} = 10 mA)			10.9	–	10.4	11.7	–	9.6	–	
(I_{OH} = 15 mA)			9.7	–	8.8	10.3	–	7.45	–	
(I_{OH} = 20 mA)			8.5	–	7.2	8.8	–	5.25	–	
(I_{OH} = 25 mA)			7.4	–	5.6	7.1	–	3.0	–	
Output Sink Current: j	I_{OL}									mA
(V_{OL} = 0.4 V)		5	–	–	0.3	1.00	–	–	–	
(V_{OL} = 0.5 V)		10	–	–	–	–	–	–	–	
(V_{OL} = 1.5 V)		15	–	–	0.5	1.25	–	–	–	
Input Current (L Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (P Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5	–	0.3	–	0.08	0.25	–	0.2	mA
V_{in} = 0 or V_{DD}, $I_{out} = 0$ μA		10	–	1.5	–	0.40	1.25	–	1.0	
(Per Package)		15	–	3.0	–	0.85	2.50	–	2.0	
Total Supply Current**†	I_T	5			$I_T = (1.9\ \mu A/kHz)f + I_{DD}$					μA
(Dynamic plus Quiescent,		10			$I_T = (3.8\ \mu A/kHz)f + I_{DD}$					
Per Package)		15			$I_T = (5.7\ \mu A/kHz)f + I_{DD}$					
(C_L = 50 pF on all outputs, all buffers switching)										

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3}(C_L - 50)\ V_{DD}f$

where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

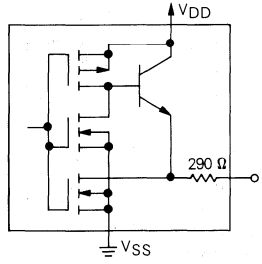
**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination. Noise margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Output Rise Time, a–g, h+i Outputs (Figure 1)	t_{TLH}					ns
		5	–	210	450	
		10	–	145	300	
		15	–	90	200	
Output Fall Time, a–g, h+i Outputs (Figure 1)	t_{THL}					μs
		5	–	1.5	3.5	
		10	–	1.3	2.75	
		15	–	1.1	2.25	
Output Fall Time, j Output (Figures 3 and 4)	t_{THL}					ns
		5	–	105	250	
		10	–	40	100	
		15	–	30	75	
Propagation Delay Time, A, B, C, D to a–g, h+i Outputs (Figure 2)	t_{PLH}					ns
		5	–	935	2400	
		10	–	340	900	
		15	–	230	500	
	t_{PHL}	5	–	7.0	18.0	μs
		10	–	3.5	9.0	
		15	–	2.0	5.0	
Propagation Delay Time, A, B, C, D to j Output (Figures 3 and 4)	t_{PLZ}					μs
		5	–	11.0	25.0	
		10	–	8.0	20.0	
		15	–	4.0	10.0	
	t_{PZL}	5	–	800	1500	ns
		10	–	400	1000	
		15	–	200	500	
Propagation Delay Time, LE to a–g, h+i Outputs (Figure 5)	t_{PLH}					ns
		5	–	1300	3000	
		10	–	500	1500	
		15	–	350	1000	
	t_{PHL}	5	–	16.0	30.0	μs
		10	–	6.0	15.0	
		15	–	5.0	10.0	
Propagation Delay Time, LE to j Output (Figures 4 and 6)	t_{PLZ}					μs
		5	–	14.0	30	
		10	–	8.0	20	
		15	–	6.0	15	
	t_{PZL}	5	–	10.0	25	μs
		10	–	5.0	15	
		15	–	4.0	10	
Setup Time, A, B, C, D to LE (Figure 7)	t_{su}	5	100	35	–	ns
		10	65	25	–	
		15	65	25	–	
Hold Time, LE to A, B, C, D (Figure 7)	t_h	5	125	45	–	ns
		10	75	30	–	
		15	75	25	–	
Latch Enable Pulse Width, LE (Figure 7)	t_w	5	525	210	–	ns
		10	200	80	–	
		15	140	55	–	

OUTPUT CIRCUIT
(Except Pin 11)



INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h+i; PINS 12, 13, 14, 15, 1, 2, 3, 4)

The segment drivers are emitter-follower NPN transistors. To limit the output current, a resistor, typically 290 ohms, is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of V_{DD} = 5.0 volts.

OUTPUT (j; PIN 11)

This open-drain output is activated (goes low) whenever inputs A, B, C, and D are all set to a logic one. Otherwise the output is in the high-impedance state. See the truth table.

INPUT DATA (A, B, C, D; PINS 5, 6, 9, 10)

The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by the Latch Enable input.

LATCH ENABLE (LE; PIN 7)

The data on inputs A, B, C and D will pass through the latch and will be decoded immediately when LE is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when LE = low and will be latched with the rising edge of LE. The data will remain stored as long as LE is high.

4

SWITCHING WAVEFORMS

Figure 1

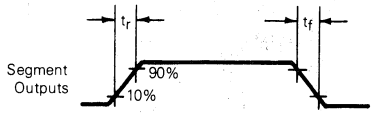


Figure 2

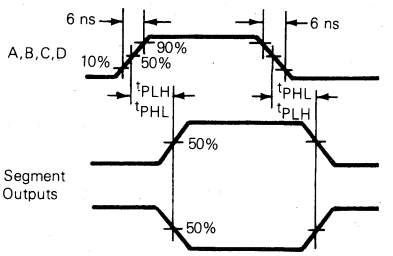


Figure 3

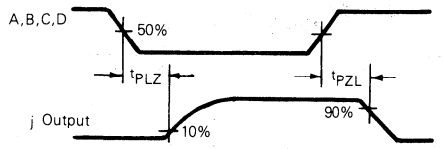


Figure 4

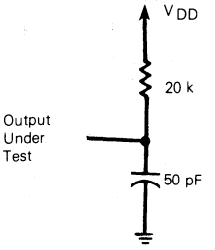
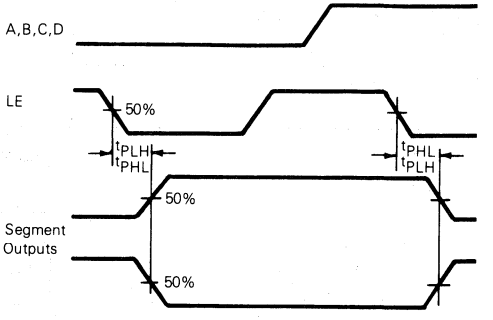


Figure 5



SWITCHING WAVEFORMS

Figure 6

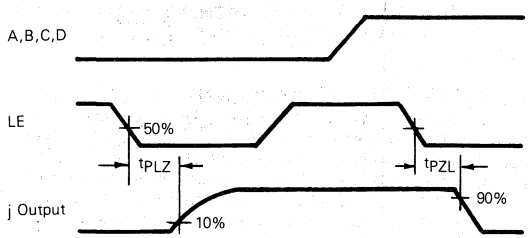
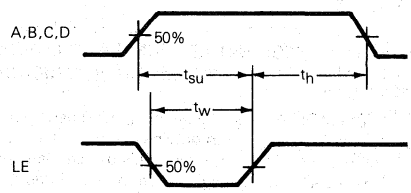
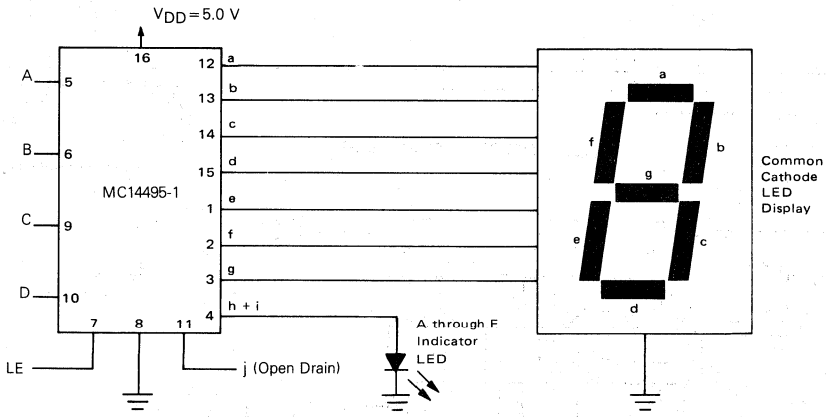


Figure 7



TYPICAL CIRCUIT @ V_{DD} = 5.0 V



MOTOROLA

MC14499

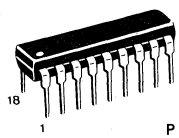
7-SEGMENT LED DISPLAY DECODER/DRIVER WITH SERIAL INTERFACE

The MC14499 is a 7-segment alphanumeric LED decoder/driver with a serial interface port to provide communication with CMOS microprocessors and microcomputers. This device features NPN output drivers which allow interfacing to common cathode LED displays through external series resistors.

- High-Current Segment Drivers on Chip
- CMOS MPU Compatible Input Levels
- Wide Operating Voltage Range: 4.5 to 6.5 V
- Drives Four Characters with Decimal Points

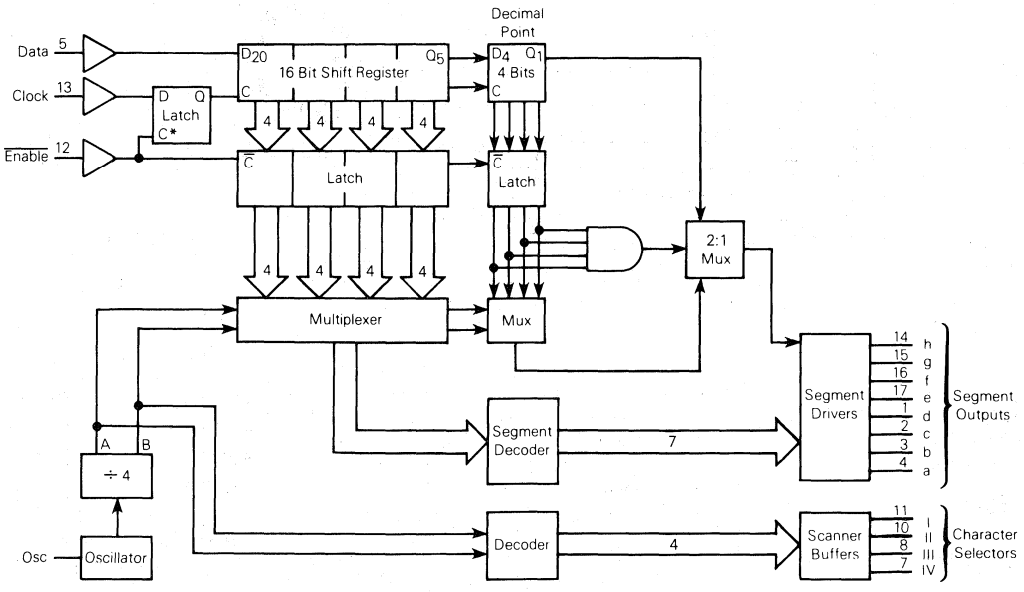
CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

7-SEGMENT LED DISPLAY DECODER/DRIVER WITH SERIAL INTERFACE



P SUFFIX
PLASTIC PACKAGE
CASE 707

FIGURE 1 — BLOCK DIAGRAM



* Transparent Latch

V_{DD} = Pin 18
V_{SS} = Pin 9

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to + 7.0	Vdc
Input Voltage, all Inputs	V_{IN}	−0.5 to V_{DD} + 0.5	Vdc
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{STG}	−65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 6.5 V)

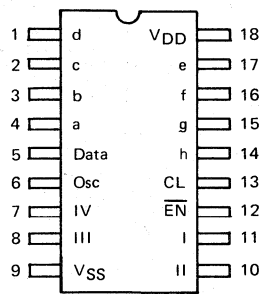
Characteristic	Pin	Symb.	0°		25°			70°		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Input Voltage '0' level	5,12,	V_{IL}		0.3xV_{DD}	–	0.45xV_{DD}	0.3xV_{DD}		0.3xV_{DD}	Vdc
'1' level	13	V_{IH}	0.7xV_{DD}		0.7xV_{DD}	0.55xV_{DD}	–	0.7xV_{DD}		Vdc
Input Current (V_{IN} = 0 to V_{DD})		I_{IN}		±0.1		±0.001	±0.1		±1.0	μA
Oscillator Input Voltage '0' level	6	V_{ILO}		0.25xV_{DD}	–	0.3xV_{DD}	0.25xV_{DD}		0.2xV_{DD}	Vdc
'1' level		V_{IHO}	0.75xV_{DD}		0.75xV_{DD}	0.7xV_{DD}	–	0.8xV_{DD}		Vdc
Oscillator Input Current V_{OSC}=0		I_{IOL}		100	30	50	80	10		μA
V_{OSC}=V_{DD}		I_{IOH}		−100	−30	−50	−80	−10		μA
Segment Driver Voltage below V_{DD}	1–4,	V_{DD}-								
I_{OUT}=50mA	14,15,	V_{SOH}		1.1	–	0.9	1.0		1.1	Vdc
I_{OUT}=10mA	16,17			0.8	–	0.7	0.75		0.8	Vdc
Segment Driver OFF Leakage		I_{OFF}								
V_{OUT} = 0				100	–	1	50		100	μA
Digit Drivers	7,8,									
Source (On) V_{OUT} = 0.8 V	10,11	I_{DOH}	6		5.5	8	–	4		mA
Sink (Off) V_{OUT} = 0.5 V		I_{DOL}	−0.2		−0.2	−2	–	−0.1		mA
Quiescent Current	18									
V_{IN} = 0, I_{OUT} = 0, C_{OSC} = 15 nF				1	–	0.5	1		1	mA
Maximum Power Dissipation				500	–	–	500		500	mW

SWITCHING CHARACTERISTICS (V_{DD} = 5V ± 10 %, T_A = 0 to 70 °C)

Characteristic	Fig.	Symbol	Min.	Max.	Unit
Clock High time	3	t_{CH}	2		μs
Clock Low time	3	t_{CL}	2		μs
Clock Rise time	3	t_{CR}		2	μs
Clock Fall time	3	t_{CF}		2	μs
Enable Lead time	3	t_{Elead}	200		ns
Enable Lag time	3	t_{Elag}	200		ns
Data Set-up time	3	t_{DSup}	200		ns
Data Hold time	3	t_{DHold}	1		μs
Scanner Frequency*	5	$1/t_{Scan}$	50	300	Hz
Osc/Digit Lead time	5	t_{OD}		10	μs
Osc/Segment Lead time	5	t_{OS}		10	μs
Digit Overlap	5	t_{OV}		5	μs

* Scanner Capacitance = 22nF.

PIN ASSIGNMENT



CIRCUIT OPERATION

The circuit accepts a 20-bit input, 16-bits for the four digit display plus 4-bits for the decimal point – these latter four-bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in figure 2.

In order to enter data the enable input, $\overline{EN}$, must be low, = 0. The sample and shift are accomplished on the falling clock edge, see figure 3. Data are loaded from the shift register to the latches when $\overline{EN}$ goes high, = 1. While the shift register is being loaded the previous data are stored in the latches.

If the decimal point is used the system requires 20 clock pulses to load data, otherwise only 16 are required.

CASCADING

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see figure 4. Therefore, to cascade n four digit display drivers a set-up is used which will firstly load the 1111 cascading word :

1 $\overline{EN} = 0$

2 Load 20-bits, the first four bits being 1, with 20 clock pulses.

3 $\overline{EN} = 1$, to load the latch

4 Repeat steps 1 to 3 (n-1) times

5 (nX20)-bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

SCANNER

The scanner frequency is determined by an on-chip oscillator, which requires an external frequency determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800Hz – to avoid flicker and digit overlap. For test purposes this frequency can be increased up to 10kHz.

A divide by four counter provides four non-over lapping scanner waveforms corresponding to the four digits – see figure 5.

SEGMENT DECODER

The code used in this matrix decoders is shown in figure 6.

OUTPUT DRIVERS

There are two different drivers :

The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.

The digit output buffers; These are short circuit protected CMOS devices.

A typical application circuit is shown in figure 7.

FIGURE 2 – INPUT SEQUENCE

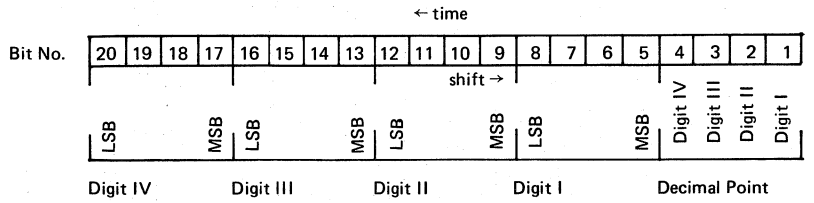


FIGURE 3a – SERIAL INPUT, POSITIVE CLOCK

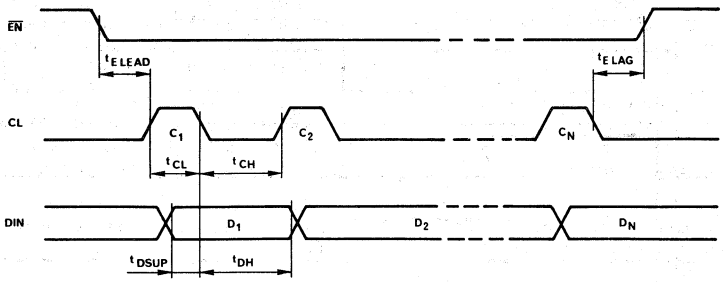


FIGURE 3b – SERIAL INPUT, NEGATIVE CLOCK

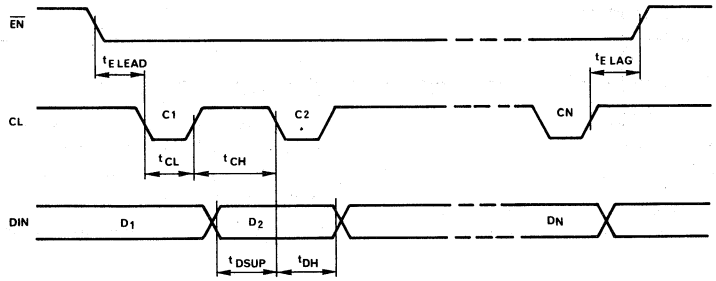


FIGURE 4 – CASCADING MC 14499s

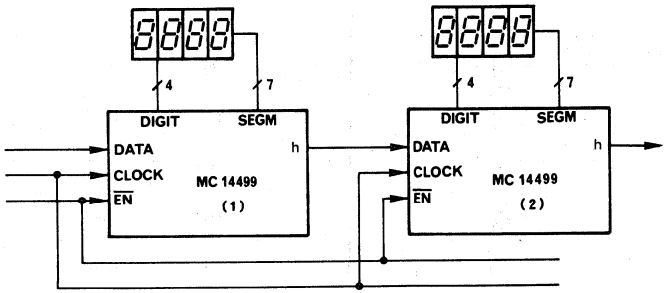


FIGURE 5 – SCANNER WAVEFORMS

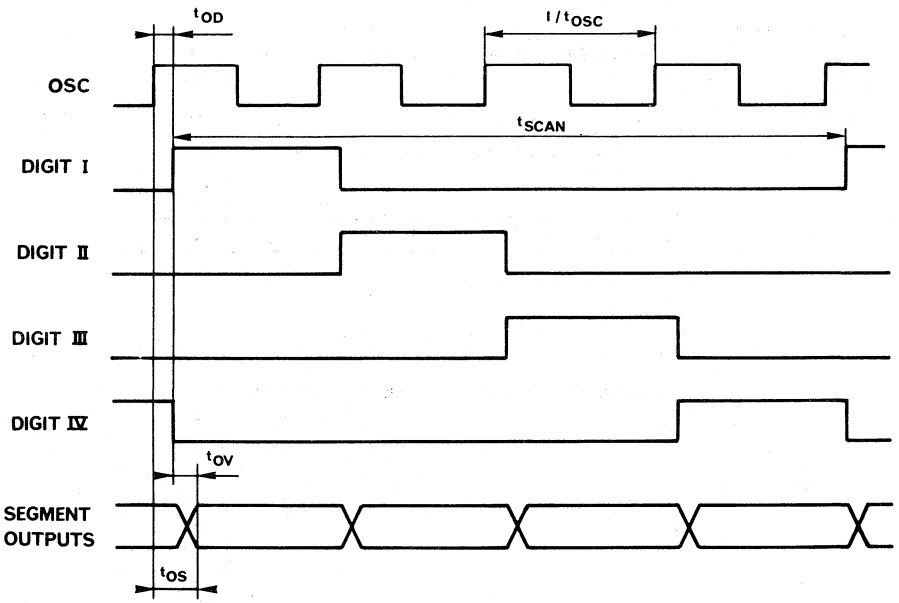


FIGURE 6 – SEGMENT CODE

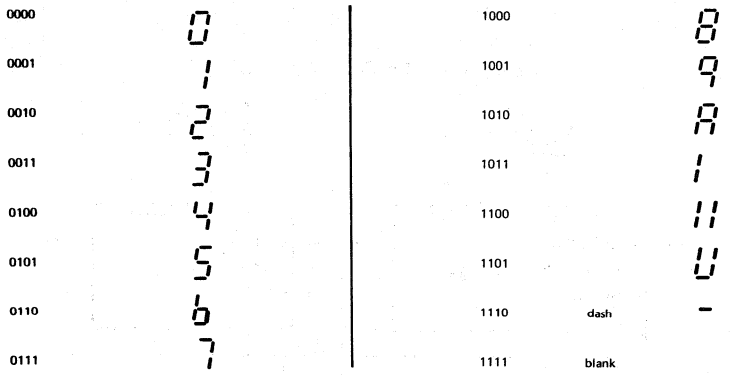
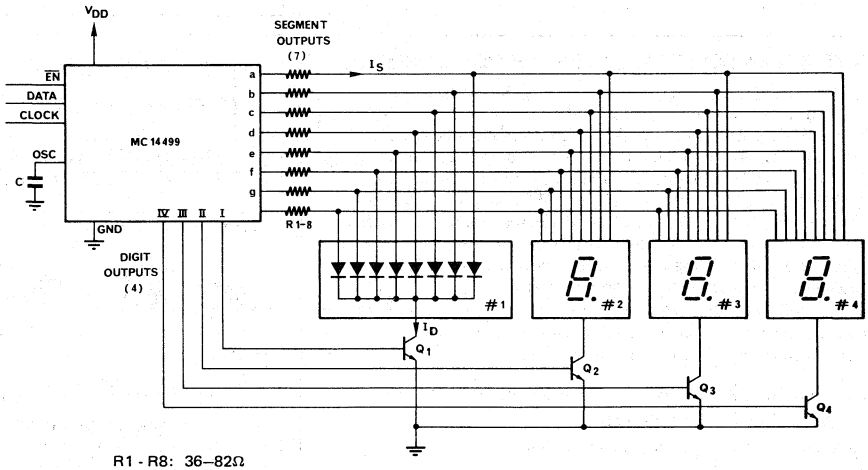


FIGURE 7 – APPLICATION EXAMPLE



R1 - R8: 36–82Ω
C: 22 nF

V_{DD} Typ: 5–6 V
I_S max.: 40–50 mA
$I_D$max.: $8I_S$ max.

4

MOTOROLA

MC14511B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 V
- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Chip Complexity: 216 FETs or 54 Equivalent Gates

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

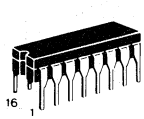
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

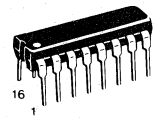
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

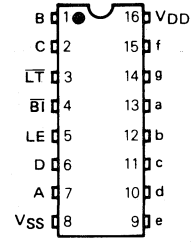


P SUFFIX
PLASTIC PACKAGE
CASE 648

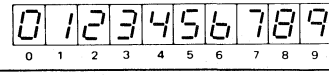
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				•				•

X = Don't Care
*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	V
$V_{in} = 0$ or V_{DD}			10	9.1	–	9.1	9.58	–	9.1	–	
			15	14.1	–	14.1	14.59	–	14.1	–	
Input Voltage#	"0" Level	V_{IL}									V
(V_O = 3.8 or 0.5 V)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 V)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 V)			15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 3.8 V)	"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 8.8 V)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 V)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Voltage (AL Device)		V_{OH}									V
(I_{OH} = 0 mA)	Source		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mA)				–	–	–	4.24	–	–	–	
(I_{OH} = 10 mA)				3.90	–	3.90	4.12	–	3.5	–	
(I_{OH} = 15 mA)				–	–	–	3.94	–	–	–	
(I_{OH} = 20 mA)				3.40	–	3.40	3.70	–	3.0	–	
(I_{OH} = 25 mA)				–	–	–	3.54	–	–	–	
(I_{OH} = 0 mA)			10	9.10	–	9.10	9.58	–	9.1	–	V
(I_{OH} = 5.0 mA)				–	–	–	9.26	–	–	–	
(I_{OH} = 10 mA)				9.00	–	9.00	9.17	–	8.6	–	
(I_{OH} = 15 mA)				–	–	–	9.04	–	–	–	
(I_{OH} = 20 mA)				8.60	–	8.60	8.90	–	8.2	–	
(I_{OH} = 25 mA)				–	–	–	8.70	–	–	–	
(I_{OH} = 0 mA)			15	14.1	–	14.1	14.59	–	14.1	–	V
(I_{OH} = 5.0 mA)				–	–	–	14.27	–	–	–	
(I_{OH} = 10 mA)				14.0	–	14.0	14.18	–	13.6	–	
(I_{OH} = 15 mA)				–	–	–	14.07	–	–	–	
(I_{OH} = 20 mA)				13.6	–	13.6	13.95	–	13.2	–	
(I_{OH} = 25 mA)				–	–	–	13.70	–	–	–	
Output Drive Voltage (CL/CP Device)		V_{OH}									V
(I_{OH} = 0 mA)	Source		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mA)				–	–	–	4.24	–	–	–	
(I_{OH} = 10 mA)				3.60	–	3.60	4.12	–	3.3	–	
(I_{OH} = 15 mA)				–	–	–	3.94	–	–	–	
(I_{OH} = 20 mA)				2.80	–	2.80	3.75	–	2.5	–	
(I_{OH} = 25 mA)				–	–	–	3.54	–	–	–	
(I_{OH} = 0 mA)			10	9.10	–	9.10	9.58	–	9.1	–	V
(I_{OH} = 5.0 mA)				–	–	–	9.26	–	–	–	
(I_{OH} = 10 mA)				8.75	–	8.75	9.17	–	8.45	–	
(I_{OH} = 15 mA)				–	–	–	9.04	–	–	–	
(I_{OH} = 20 mA)				8.10	–	8.10	8.90	–	7.8	–	
(I_{OH} = 25 mA)				–	–	–	8.75	–	–	–	
(I_{OH} = 0 mA)			15	14.1	–	14.1	14.59	–	14.1	–	V
(I_{OH} = 5.0 mA)				–	–	–	14.27	–	–	–	
(I_{OH} = 10 mA)				13.75	–	13.75	14.18	–	13.45	–	
(I_{OH} = 15 mA)				–	–	–	14.07	–	–	–	
(I_{OH} = 20 mA)				13.1	–	13.1	13.95	–	12.8	–	
(I_{OH} = 25 mA)				–	–	–	13.80	–	–	–	
Output Drive Current (AL Device)		I_{OL}									mA
(V_{OL} = 0.4 V)	Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 V)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OL}									mA
(V_{OL} = 0.4 V)	Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	3.6	–	3.0	8.8	–	2.4	–	

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package) V_{in}=0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Quiescent Current (CL/CP Device) (Per Package) V_{in}=0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0 10 15	— — —	20 40 80	— — —	0.005 0.010 0.015	20 40 80	— — —	150 300 600	μA
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.9 μA/kHz) f + I_{DD} I_T = (3.8 μA/kHz) f + I_{DD} I_T = (5.7 μA/kHz) f + I_{DD}							μA

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		5.0	—	40	80	
t_{TLH} = (0.25 ns/pF) C_L + 17.5 ns		10	—	30	60	
t_{TLH} = (0.20 ns/pF) C_L + 15 ns		15	—	25	50	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	—	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	—	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	—	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	—	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	—	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	—	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	—	720	1440	
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	—	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	—	200	400	
Blank Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 585 ns		5.0	—	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 187.5 ns		10	—	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 142.5 ns		15	—	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	—	485	970	
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	—	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	—	160	320	
Lamp Test Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	—	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	—	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	—	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	—	313	625	
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	—	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	—	90	180	
Setup Time	t_{su}	5.0	100	—	—	ns
		10	40	—	—	
		15	30	—	—	
Hold Time	t_h	5.0	60	—	—	ns
		10	40	—	—	
		15	30	—	—	
Latch Enable Pulse Width	t_{WL}	5.0	520	260	—	ns
		10	220	110	—	
		15	130	65	—	

*The formulas given are for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

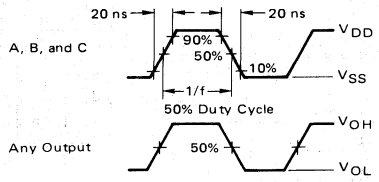
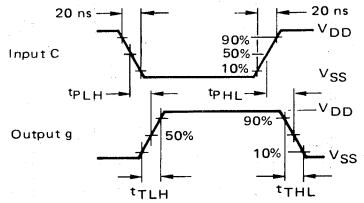
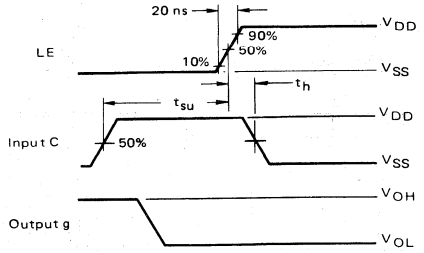


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

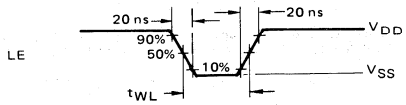
(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

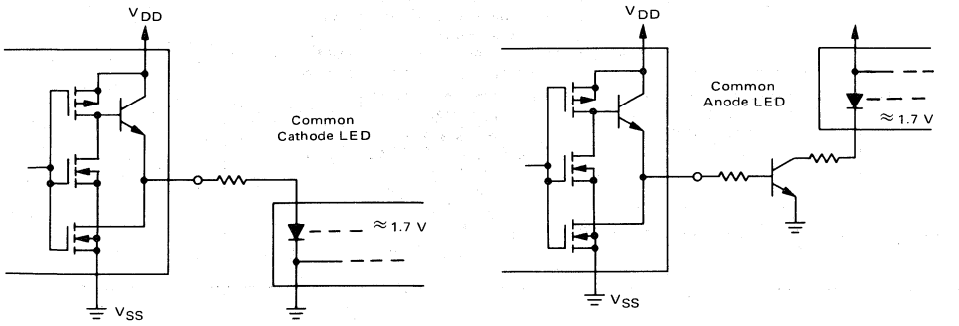


(c) Data DCBA strobed into latches.

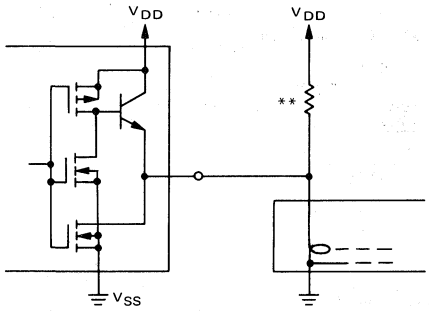


CONNECTIONS TO VARIOUS DISPLAY READOUTS

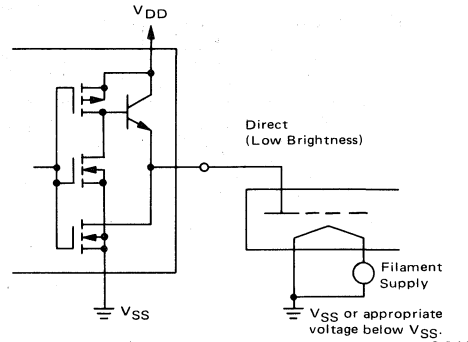
LIGHT EMITTING DIODE (LED) READOUT



INCANDESCENT READOUT

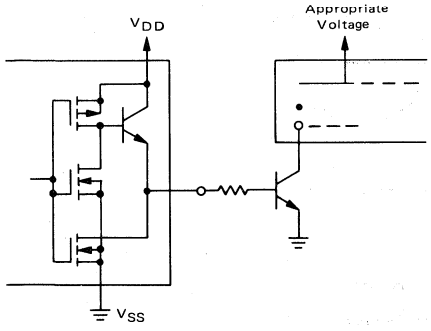


FLUORESCENT READOUT

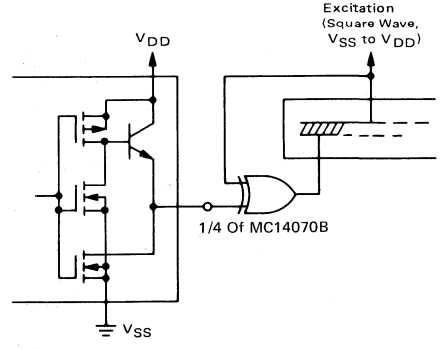


(CAUTION: Maximum working voltage = 18.0 V)

GAS DISCHARGE READOUT



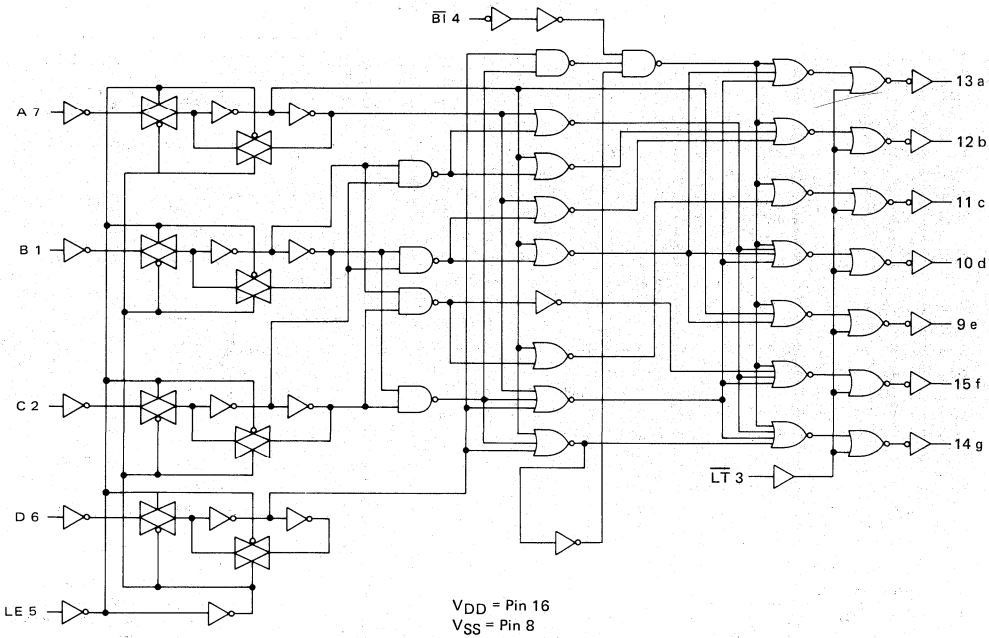
LIQUID CRYSTAL (LCD) READOUT



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MOTOROLA

MC14513B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and has output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

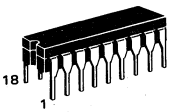
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 V
- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

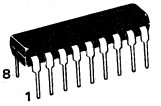
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



L SUFFIX
CERAMIC PACKAGE
CASE **726**

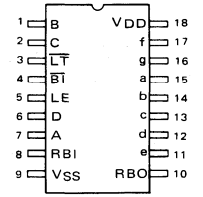


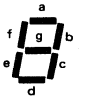
P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT





DISPLAY

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (see Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS								OUTPUTS							
RBI	LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	X	0	X	X	X	X	#	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	#	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	=			*					*

X = *Don't Care*
= RBO = RBI ($\overline{D}\,\overline{C}\,\overline{B}\,\overline{A}$), indicated by other rows of table.
* Depends upon the BCD code previously applied when LE = 0.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage — Segment Outputs	V_{OL}									V
"0" Level		5.0	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.1	–	4.1	5.0	–	4.1	–	V
V_{in} = 0 or V_{DD}		10	9.1	–	9.1	10	–	9.1	–	
		15	14.1	–	14.1	15	–	14.1	–	
Output Voltage — RBO Output	V_{OL}									V
"0" Level		5.0	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									V
(V_O = 3.8 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 3.8 V) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 8.8 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Voltage — Segments (AL Device)	V_{OH}									V
(I_{OH} = 0 mA) Source:		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mA)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mA)			3.90	–	3.90	4.12	–	3.5	–	
(I_{OH} = 15 mA)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mA)			3.40	–	3.40	3.75	–	3.0	–	
(I_{OH} = 25 mA)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mA)		10	9.10	–	9.10	9.58	–	9.1	–	V
(I_{OH} = 5.0 mA)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mA)			9.00	–	9.00	9.17	–	8.6	–	
(I_{OH} = 15 mA)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mA)			8.60	–	8.60	8.90	–	8.2	–	
(I_{OH} = 25 mA)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mA)		15	14.1	–	14.1	14.59	–	14.1	–	V
(I_{OH} = 5.0 mA)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mA)			14.0	–	14.0	14.18	–	13.6	–	
(I_{OH}=15 mA)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mA)			13.6	–	13.6	13.95	–	13.2	–	
(I_{OH} = 25 mA)			–	–	–	13.80	–	–	–	
Output Drive Voltage — Segments (CL/CP Device)	V_{OH}									V
(I_{OH} = 0 mA) Source:		5.0	4.10	–	4.10	4.57	–	4.1	–	
(I_{OH} = 5.0 mA)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mA)			3.60	–	3.60	4.12	–	3.3	–	
(I_{OH} = 15 mA)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mA)			2.80	–	2.80	3.75	–	2.5	–	
(I_{OH} = 25 mA)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mA)		10	9.10	–	9.10	9.58	–	9.1	–	V
(I_{OH} = 5.0 mA)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mA)			8.75	–	8.75	9.17	–	8.45	–	
(I_{OH} = 15 mA)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mA)			8.10	–	8.10	8.90	–	7.8	–	
(I_{OH} = 25 mA)			–	–	–	8.75	–	–	–	
(I_{OH} = 0 mA)		15	14.1	–	14.1	14.59	–	14.1	–	V
(I_{OH} = 5.0 mA)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mA)			13.75	–	13.75	14.18	–	13.45	–	
(I_{OH} = 15 mA)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mA)			13.1	–	13.1	13.95	–	12.8	–	
(I_{OH} = 25 mA)			–	–	–	13.80	–	–	–	

4

ELECTRICAL CHARACTERISTICS (Continued)

	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Drive Current – RBO Output (AL Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	-0.40	–	-0.32	-0.64	–	-0.22	–	
(V_{OH} = 9.5 V)		10	-0.21	–	-0.17	-0.34	–	-0.12	–	
(V_{OH} = 13.5 V)		15	-0.81	–	-0.66	-1.3	–	-0.46	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.18	–	0.15	0.29	–	0.10	–	mA
(V_{OL} = 0.5 V)		10	0.47	–	0.38	0.75	–	0.26	–	
(V_{OL} = 1.5 V)		15	1.8	–	1.5	2.9	–	1.0	–	
Output Drive Current – RBO Output (CL/CP Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	-0.25	–	-0.21	-0.64	–	-0.17	–	
(V_{OH} = 9.5 V)		10	-0.13	–	-0.11	-0.34	–	-0.092	–	
(V_{OH} = 13.5 V)		15	-0.52	–	-0.44	-1.3	–	-0.36	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.12	–	0.098	0.29	–	0.080	–	mA
(V_{OL} = 0.5 V)		10	0.30	–	0.25	0.75	–	0.21	–	
(V_{OL} = 1.5 V)		15	1.2	–	0.98	2.9	–	0.80	–	
Output Drive Current – Segments (AL Device)	I_{OL}									mA
(V_{OL} = 0.4 V) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 V)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current – Segments (CL/CP Device)	I_{OL}									mA
(V_{OL} = 0.4 V) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µA
(Per Package) V_{in} = 0 or V_{DD},		10	–	10	–	0.010	10	–	300	
I_{out} = 0 µA		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µA
(Per Package) V_{in} = 0 or V_{DD},		10	–	40	–	0.010	40	–	300	
I_{out} = 0 µA		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 µA/kHz) f + I_{DD}							µA
		10	I_T = (3.8 µA/kHz) f + I_{DD}							
		15	I_T = (5.7 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +25°C for CL/CP Device.

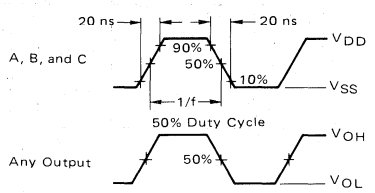
Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

† To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

** The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

Input LE and RBI low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.



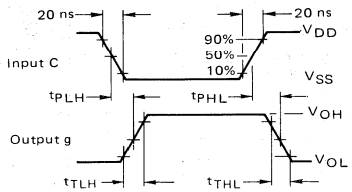
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise Time – Segment Outputs	t_{TLH}					ns
		5.0	–	40	80	
		10	–	30	60	
		15	–	25	50	
Output Rise Time – RBO Output	t_{TLH}					ns
		5.0	–	480	960	
		10	–	240	480	
		15	–	190	380	
Output Fall Time–Segment Outputs*	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Output Fall Time – RBO Outputs	t_{THL}					ns
t_{THL} = (3.25 ns/pF) C_L + 107.5 ns		5.0	–	270	540	
t_{THL} = (1.35 ns/pF) C_L + 67.5 ns		10	–	135	270	
t_{THL} = (0.95 ns/pF) C_L + 62.5 ns		15	–	110	220	
Propagation Delay Time–A, B, C, D Inputs*	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	–	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Propagation Delay Time–RBI and $\overline{BI}$ Inputs*	t_{PLH}					ns
t_{PLH} = (1.05 ns/pF) C_L + 547.5 ns		5.0	–	600	750	
t_{PLH} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	300	
t_{PLH} = (0.30 ns/pF) C_L + 135 ns		15	–	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Propagation Delay Time–$\overline{LT}$ Input*	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	–	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	–	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	–	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	–	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	–	90	180	
Setup Time	t_{su}	5.0	100	–	–	ns
		10	40	–	–	
		15	30	–	–	
Hold Time	t_h	5.0	60	–	–	ns
		10	40	–	–	
		15	30	–	–	
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0	520	260	–	ns
		10	220	110	–	
		15	130	65	–	

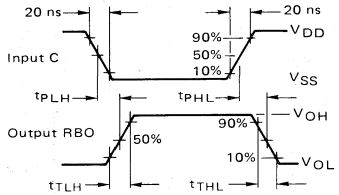
*The formulas given are for the typical characteristics only.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

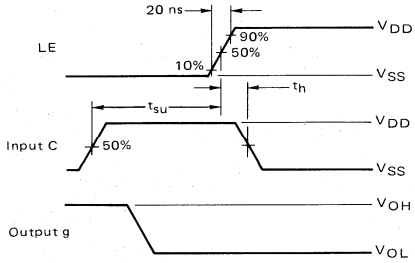
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



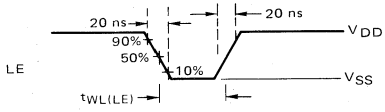
b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{BI}$ and $\overline{LT}$ high.



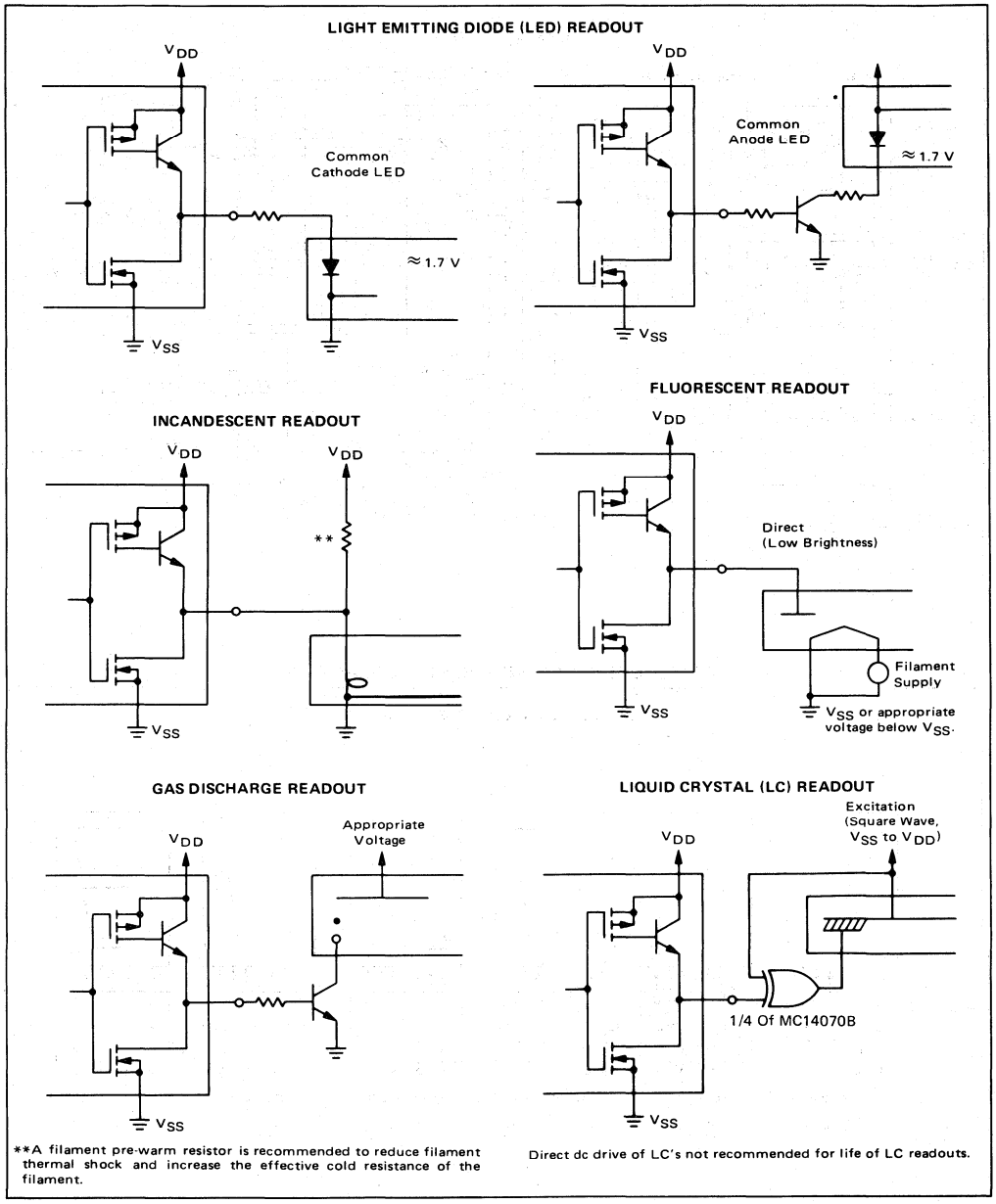
c. Setup and Hold Times: Input RBI and D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



d. Pulse Width: Data DCBA strobed into latches.



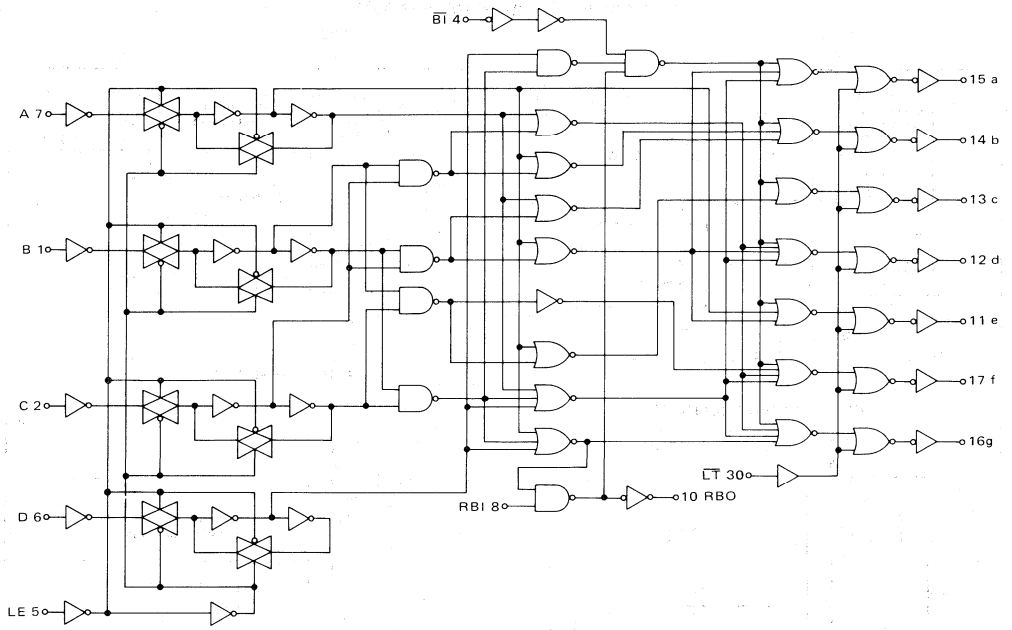
CONNECTIONS TO VARIOUS DISPLAY READOUTS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

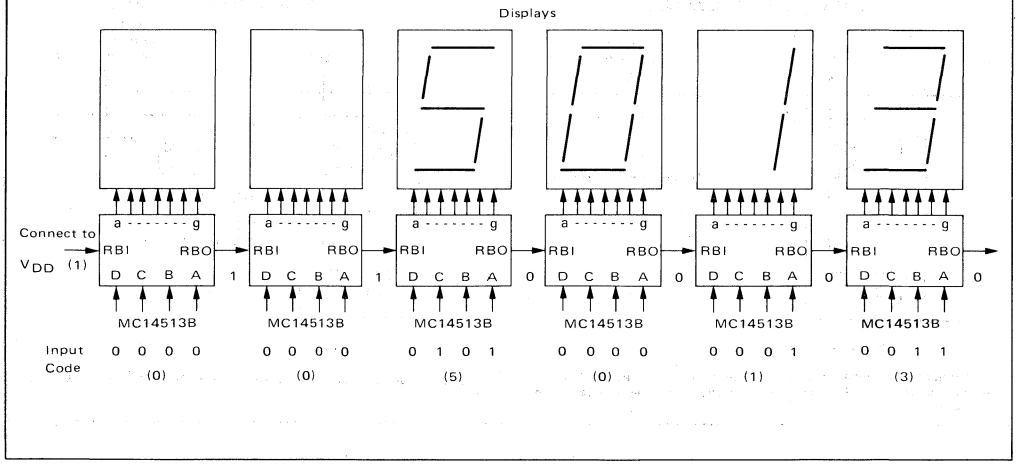
Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM



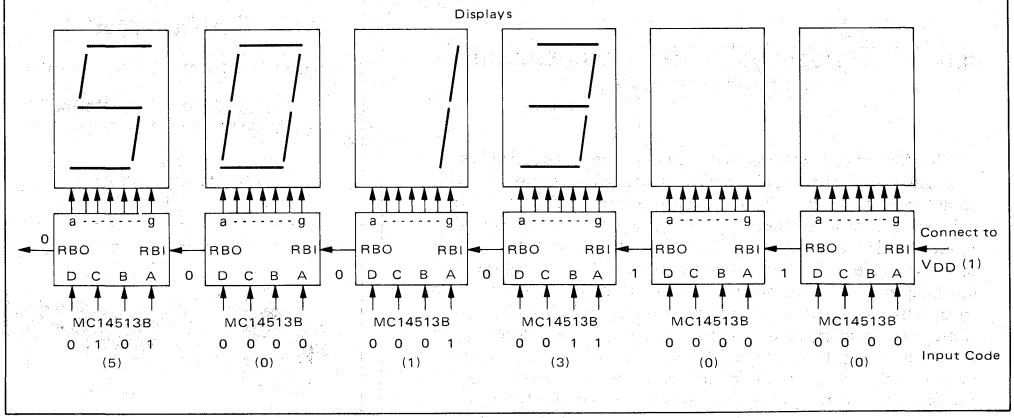
TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont)

TRAILING EDGE ZERO SUPPRESSION



MOTOROLA

MC14543B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

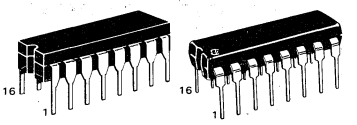
BCD-TO-SEVEN SEGMENT
LATCH/DECODER/DRIVER
for
LIQUID CRYSTALS

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0 nA/package Typical @ 5 V
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).
- Chip Complexity: 207 FETs or 52 Equivalent Gates



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Rance	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mA
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

TRUTH TABLE

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X				**				**
†	†	1			†		Inverse of Output Combinations Above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15		0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	
(V_{OH} = 4.6 V)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V_{OH} = 0.5 V)		10	–	–	–	–10.1	–	–	–	
(V_{OH} = 9.5 V)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 V)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 9.5 V)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	–2.5	–	–2.1	–4.2	–	–1.7	–	
(V_{OH} = 4.6 V)		5.0	–0.52	–	–0.44	–0.88	–	–0.36	–	
(V_{OH} = 0.5 V)		10	–	–	–	–10.1	–	–	–	
(V_{OH} = 9.5 V)		10	–1.3	–	–1.1	–2.25	–	–0.9	–	
(V_{OH} = 13.5 V)		15	–3.6	–	–3.0	–8.8	–	–2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 9.5 V)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µA
(Per Package) V_{in}=0 or V_{DD},		10	–	10	–	0.010	10	–	300	
I_{out} = 0 µA		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µA
(Per Package) V_{in}=0 or V_{DD},		10	–	40	–	0.010	40	–	300	
I_{out} = 0 µA		15	–	80	–	0.015	80	–	600	
Total Supply Current**†	I_T	5.0	I_T=(1.6 µA/kHz) f + I_{DD}							µA
(Dynamic plus Quiescent,		10	I_T=(3.1 µA/kHz) f + I_{DD}							
Per Package)		15	I_T=(4.7 µA/kHz) f + I_{DD}							
(C_L=50 pF on all outputs, all buffers switching)										

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	–	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	495	
Setup Time	t_{su}	5.0	350	–	–	ns
		10	450	–	–	
		15	500	–	–	
Hold Time	t_h	5.0	40	–	–	ns
		10	30	–	–	
		15	20	–	–	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

*The formulas given are for the typical characteristics only.

4

LOGIC DIAGRAM

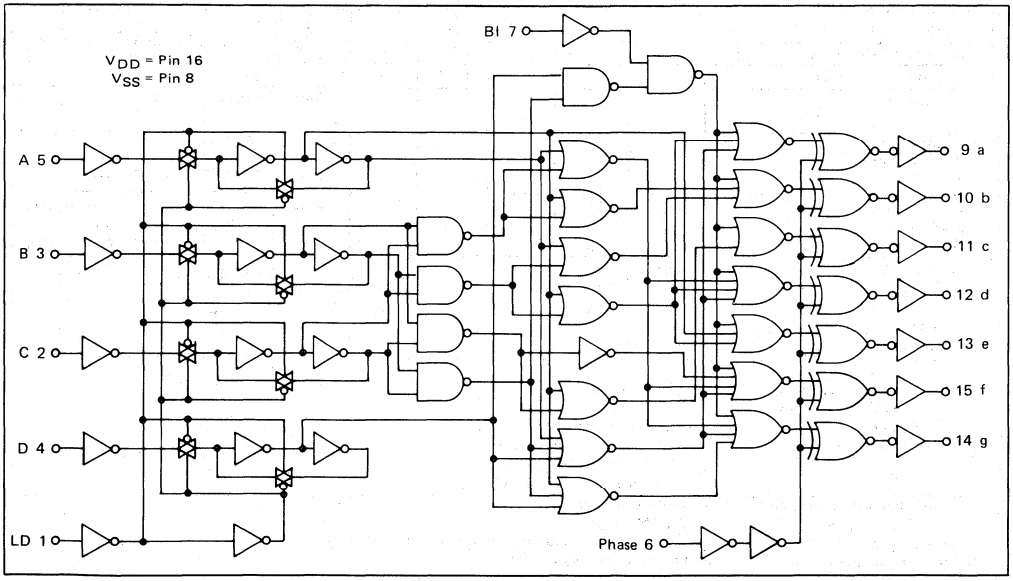


FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

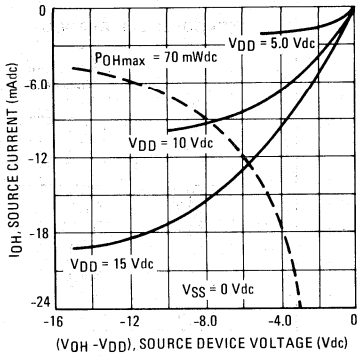
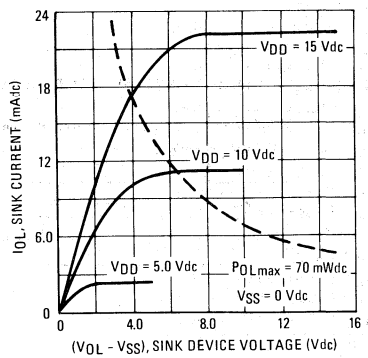


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS



4

FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

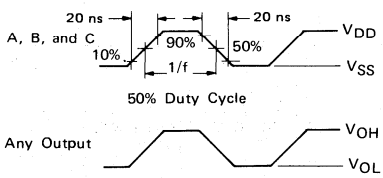
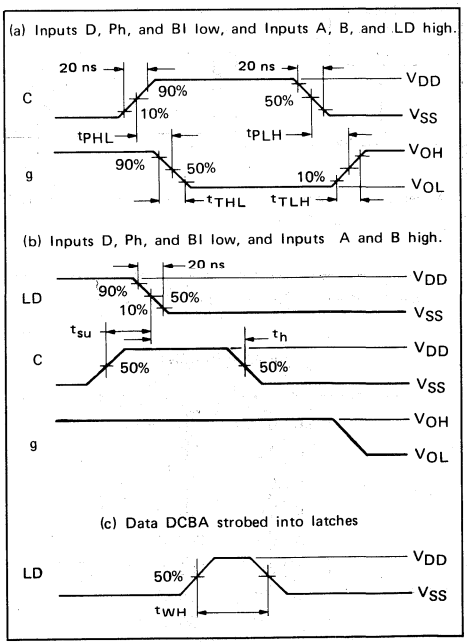
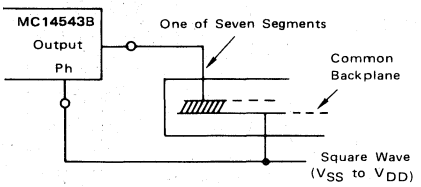


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

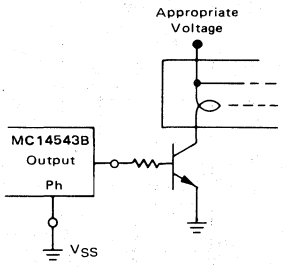


CONNECTIONS TO VARIOUS DISPLAY READOUTS

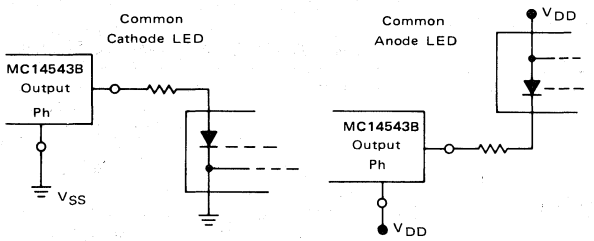
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

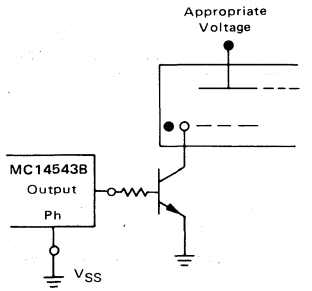


LIGHT EMITTING DIODE (LED) READOUT

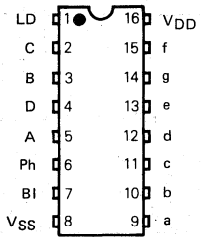


Note: Bipolar transistors may be added for gain (for $V_{DD} \leqslant 10V$ or $I_{out} \geqslant 10$ mA).

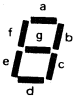
GAS DISCHARGE READOUT



PIN ASSIGNMENT

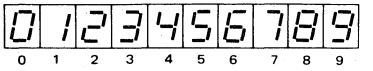


CONNECTIONS TO SEGMENTS



V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY



MOTOROLA

MC14544B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER FOR LIQUID CRYSTALS

The MC14544B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0 nA/package typical @ 5 V
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capability for Suppression of Non-significant zero
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

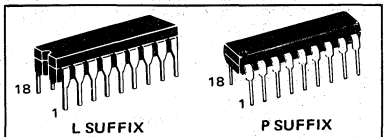
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Input Current per Pin	I_{in}	±10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING



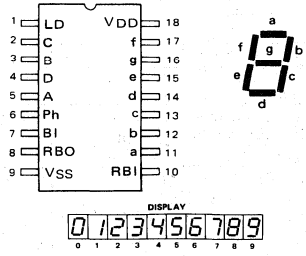
L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

4

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	
(V_{OH} = 4.6 V)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V_{OH} = 0.5 V)		10	–	–	–	–10.1	–	–	–	
(V_{OH} = 9.5 V)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 V)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 9.5 V)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	–2.5	–	–2.1	–4.2	–	–1.7	–	
(V_{OH} = 4.6 V)		5.0	–0.52	–	–0.44	–0.88	–	–0.36	–	
(V_{OH} = 0.5 V)		10	–	–	–	–10.1	–	–	–	
(V_{OH} = 9.5 V)		10	–1.3	–	–1.1	–2.25	–	–0.9	–	
(V_{OH} = 13.5 V)		15	–3.6	–	–3.0	–8.8	–	–2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 9.5 V)		10	–	–	–	10.1	–	–	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance	C_{in}	—	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µA
(Per Package) V_{in}=0 or V_{DD},		10	–	10	–	0.010	10	–	300	
I_{out} = 0 µA		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µA
(Per Package) V_{in}=0 or V_{DD},		10	–	40	–	0.010	40	–	300	
I_{out} = 0 µA		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 µA/kHz) f + I_{DD}							µA
		10	I_T = (3.1 µA/kHz) f + I_{DD}							
		15	I_T = (4.7 µA/kHz) f + I_{DD}							

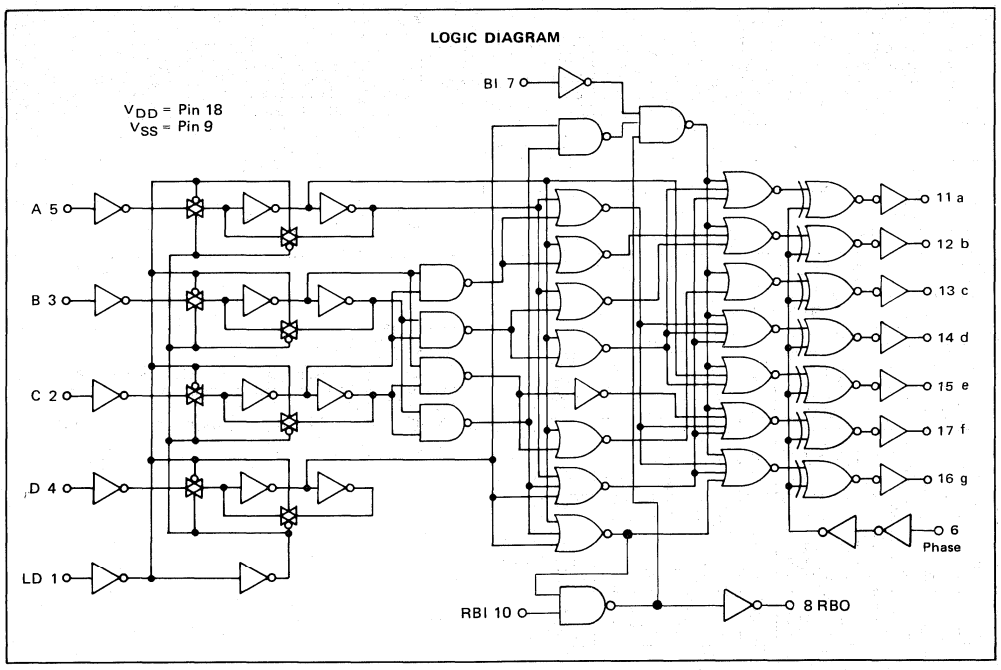
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 520 ns		5.0	–	605	1210	
t_{PLH} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1650	
t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	660	
t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	495	
Setup Time	t_{su}	5.0	0	-40	–	ns
		10	0	-15	–	
		15	0	-10	–	
Hold Time	t_h	5.0	80	40	–	ns
		10	30	15	–	
		15	20	10	–	
Latch Disable Pulse Width (Strobing Data)	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

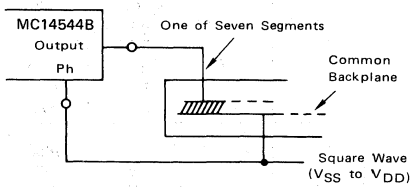
*The formulas given are for the typical characteristics only.

LOGIC DIAGRAM

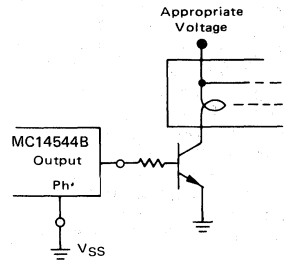


CONNECTIONS TO VARIOUS DISPLAY READOUTS

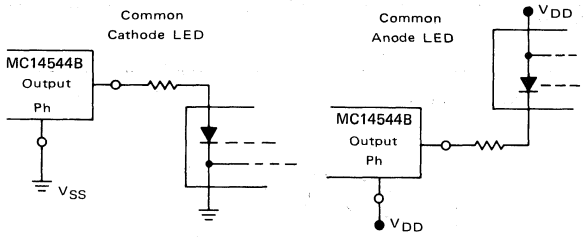
LIQUID CRYSTAL (LC) READOUT



INCANDESCENT READOUT

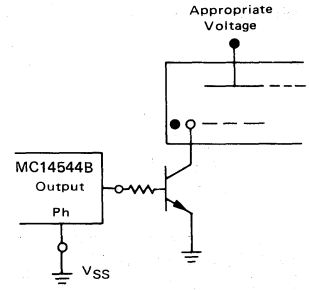


LIGHT EMITTING DIODE (LED) READOUT



Note: Bipolar transistors may be added for gain (for $V_{DD} \leqslant 10V$ or $I_{out} \geqslant 10$ mA).

GAS DISCHARGE READOUT



TRUTH TABLE

INPUTS								OUTPUTS								
RBI	LD	BI	Ph*	D	C	B	A	RBO	a	b	c	d	e	f	g	DISPLAY
X	X	1	0	X	X	X	X	=	0	0	0	0	0	0	0	Blank
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
X	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1
X	1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	2
X	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
X	1	0	0	0	1	0	0	0	0	1	1	0	0	1	1	4
X	1	0	0	0	1	0	1	0	1	0	1	1	0	1	1	5
X	1	0	0	0	1	1	0	0	1	0	1	1	1	1	1	6
X	1	0	0	0	1	1	1	0	1	1	1	0	0	0	0	7
X	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	8
X	1	0	0	1	0	0	1	0	1	1	1	1	0	1	1	9
X	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	0	0	0	X	X	X	X	=	**							**
†	†	†	1	†				†	Inverse of Output Combinations Above							Display as above

X Don't Care

† Above Combinations

* For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.

** Depends upon the BCD Code previously applied when LD = 1.

\# RBO=RBI • ($\overline{A}\overline{B}\overline{C}\overline{D}$)

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

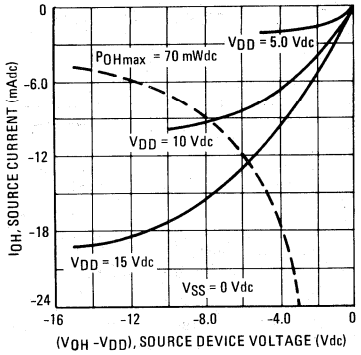
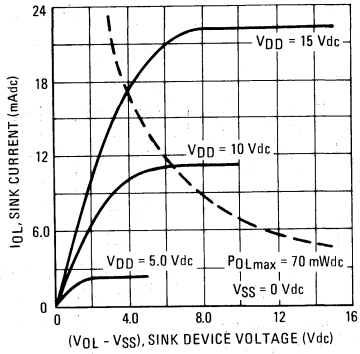


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS



4

FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

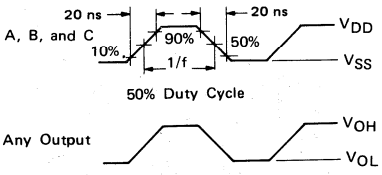
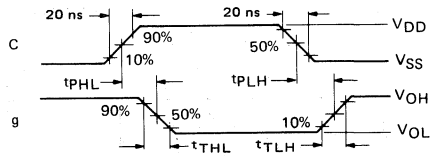
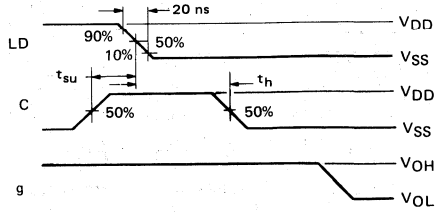


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

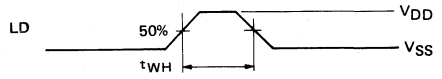
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.

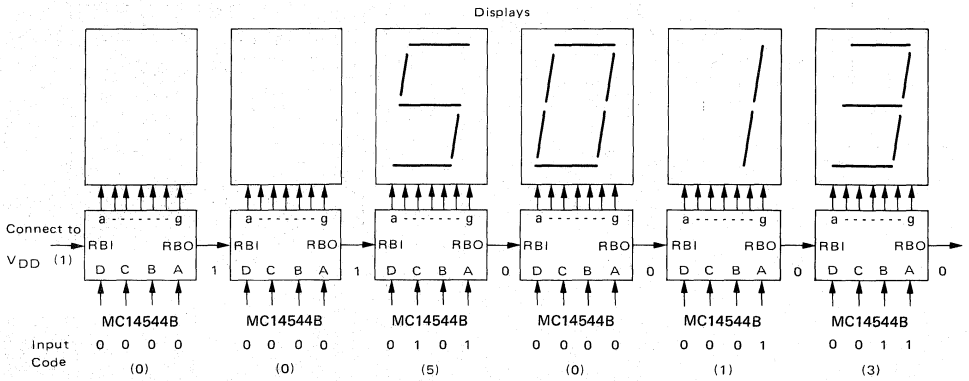


(c) Data DCBA strobed into latches

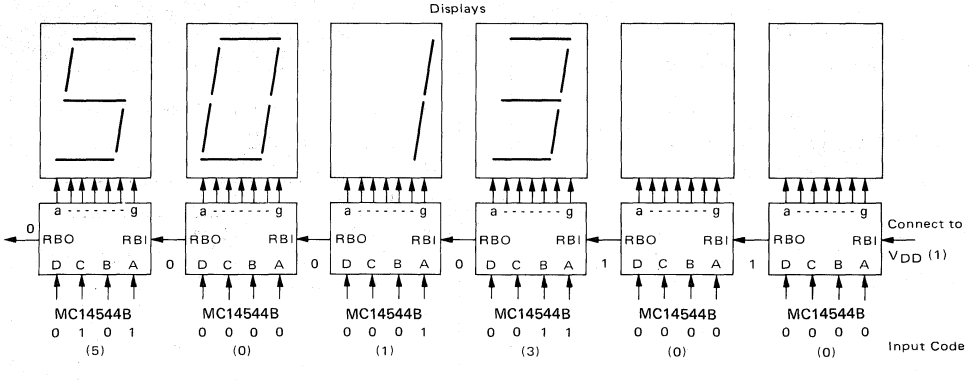


TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



TRAILING EDGE ZERO SUPPRESSION



MOTOROLA

MC14547B

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

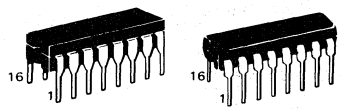
HIGH CURRENT BCD-TO-SEVEN SEGMENT DECODER/DRIVER

HIGH CURRENT BCD-TO-SEVEN SEGMENT DECODER/DRIVER

The MC14547 BCD-to-seven segment decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of an 8421 BCD-to-seven segment decoder with high output drive capability. Blanking (BI), can be used to turn off or pulse modulate the brightness of the display. The MC14547 can drive seven-segment light-emitting diodes (LED), incandescent, fluorescent or gas discharge readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- High Current Sourcing Outputs (Up to 65 mA)
- Low Logic Circuit Power Dissipation
- Supply Voltage Range = +3.0 V to +18 V
- Blanking Input
- Readout Blanking on All Illegal Combinations
- Lamp Intensity Modulation Capability
- Multiplexing Capability
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- Use MC14511B for Applications Requiring Data Latches

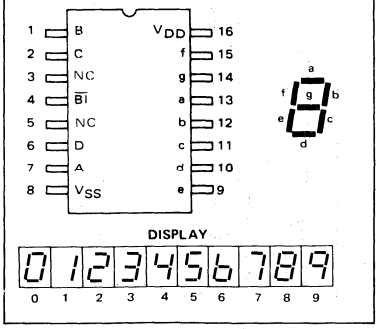


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



MAXIMUM RATINGS ★ (Voltage referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
Operating Temperature Range MC14547BAL MC14547BCL/CP	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	65	mA
Maximum Continuous Power Dissipation	P_{OHmax}	1200*	mW

★ Maximum Ratings are those values beyond which damage to the device may occur.

*See power derating curve (Figure 1).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{BI}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	1	1	0	0	1	3
1	0	1	0	0	0	1	1	0	0	1	1	4
1	0	1	0	1	1	0	1	1	0	1	1	5
1	0	1	1	0	0	0	1	1	1	1	1	6
1	0	1	1	1	1	1	1	0	0	0	0	7
1	1	0	0	0	1	1	1	1	1	1	1	8
1	1	0	0	1	1	1	1	0	0	1	1	9
1	1	0	1	0	0	0	0	0	0	0	0	Blank
1	1	0	1	1	0	0	0	0	0	0	0	Blank
1	1	1	0	0	0	0	0	0	0	0	0	Blank
1	1	1	0	1	0	0	0	0	0	0	0	Blank
1	1	1	1	0	0	0	0	0	0	0	0	Blank
1	1	1	1	1	0	0	0	0	0	0	0	Blank

X = Don't care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.1	–	4.4	4.6	–	4.3	–	V
V_{in} = 0 or V_{DD}			10	9.1	–	9.4	9.6	–	9.3	–	
			15	14.1	–	14.4	14.6	–	14.4	–	
Input Voltage #	"0" Level	V_{IL}									V
(V_O = 3.8 or 0.5 V)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 8.8 or 1.0 V)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.8 or 1.5 V)			15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 3.8 V)	"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 8.8 V)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.8 V)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Voltage (AL Device)		V_{OH}	5.0								V
(I_{OH} = 5.0 mA)	Source			4.0	–	4.2	4.3	–	4.3	–	
(I_{OH} = 10 mA)				–	–	4.1	4.3	–	–	–	
(I_{OH} = 20 mA)				3.8	–	3.9	4.2	–	4.0	–	
(I_{OH} = 40 mA)				–	–	3.7	4.0	–	–	–	
(I_{OH} = 65 mA)				3.1	–	3.2	3.7	–	3.0	–	
(I_{OH} = 5.0 mA)			10	9.1	–	9.2	9.3	–	9.3	–	
(I_{OH} = 10 mA)				–	–	9.1	9.3	–	–	–	
(I_{OH} = 20 mA)				8.8	–	9.0	9.2	–	9.2	–	
(I_{OH} = 40 mA)				–	–	8.9	9.0	–	–	–	
(I_{OH} = 65 mA)				8.4	–	8.5	8.8	–	8.1	–	
(I_{OH} = 5.0 mA)			15	14.0	–	14.2	14.3	–	14.4	–	
(I_{OH} = 10 mA)				–	–	14.1	14.3	–	–	–	
(I_{OH} = 20 mA)				13.8	–	14.0	14.2	–	14.2	–	
(I_{OH} = 40 mA)				–	–	13.8	14.0	–	–	–	
(I_{OH} = 65 mA)				13.5	–	13.5	13.7	–	13.3	–	
Output Drive Voltage (CL/CP Device)		V_{OH}	5.0								V
(I_{OH} = 5.0 mA)	Source			3.9	–	4.1	4.3	–	4.2	–	
(I_{OH} = 10 mA)				–	–	4.0	4.3	–	–	–	
(I_{OH} = 20 mA)				3.6	–	3.8	4.2	–	3.9	–	
(I_{OH} = 40 mA)				–	–	3.5	4.0	–	–	–	
(I_{OH} = 65 mA)				3.0	–	3.0	3.7	–	2.9	–	
(I_{OH} = 5.0 mA)			10	8.9	–	9.1	9.3	–	9.2	–	
(I_{OH} = 10 mA)				–	–	9.0	9.3	–	–	–	
(I_{OH} = 20 mA)				8.6	–	8.8	9.2	–	9.0	–	
(I_{OH} = 40 mA)				–	–	8.5	9.0	–	–	–	
(I_{OH} = 65 mA)				8.0	–	8.1	8.8	–	8.0	–	
(I_{OH} = 5.0 mA)			15	13.9	–	14.1	14.3	–	14.2	–	
(I_{OH} = 10 mA)				–	–	14.0	14.3	–	–	–	
(I_{OH} = 20 mA)				13.6	–	13.8	14.2	–	14.0	–	
(I_{OH} = 40 mA)				–	–	13.5	14.0	–	–	–	
(I_{OH} = 65 mA)				13.0	–	13.0	13.7	–	13.0	–	
Output Drive Current (AL Device)		I_{OL}									mA
(V_{OL} = 0.4 V)	Sink		5.0	0.32	–	0.26	0.44	–	0.18	–	
(V_{OL} = 0.5 V)			10	0.80	–	0.65	1.13	–	0.45	–	
(V_{OL} = 1.5 V)			15	2.10	–	1.7	4.4	–	1.2	–	
Output Drive Current (CL/CP Device)		I_{OL}									mA
(V_{OL} = 0.4 V)	Sink		5.0	0.26	–	0.22	0.44	–	0.18	–	
(V_{OL} = 0.5 V)			10	0.65	–	0.55	1.13	–	0.45	–	
(V_{OL} = 1.5 V)			15	1.8	–	1.5	4.4	–	1.2	–	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package) $V_{in}=0$ or V_{DD}, $I_{out}=0$ μA	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μA
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package) $V_{in}=0$ or V_{DD}, $I_{out}=0$ μA	I_{DD}	5.0	–	20	–	0.005	20	–	150	μA
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.9\ \mu A/kHz)\ f + I_{DD}$							μA
		10	$I_T = (3.8\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.7\ \mu A/kHz)\ f + I_{DD}$							

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

† To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3}(C_L - 50)\ V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

** The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	40	80	ns
		10	–	40	80	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	125	250	ns
		10	–	75	150	
		15	–	70	140	
Data Propagation Delay Time	t_{PLH}	5.0	–	750	1500	ns
		10	–	300	600	
		15	–	200	400	
	t_{PHL}	5.0	–	750	1500	
		10	–	300	600	
		15	–	200	400	
Blank Propagation Delay Time	t_{PLH}	5.0	–	750	1500	ns
		10	–	300	600	
		15	–	200	400	
	t_{PHL}	5.0	–	500	1000	
		10	–	250	500	
		15	–	170	340	

LOGIC DIAGRAM

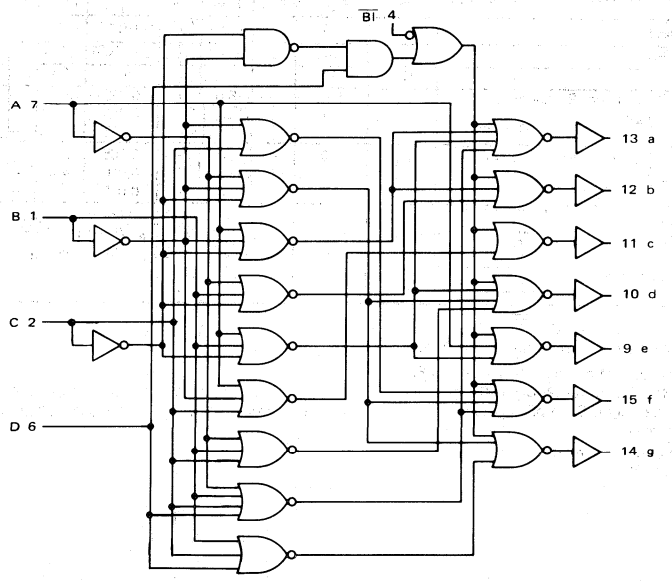
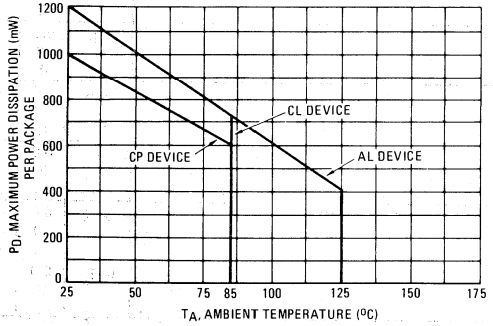
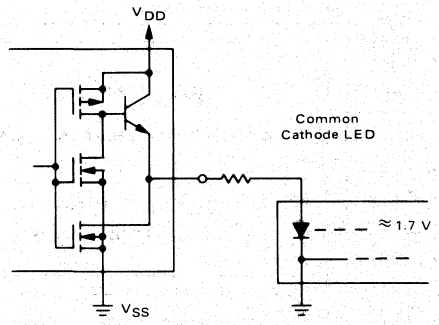


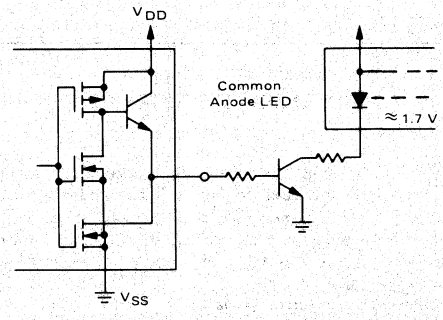
FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING



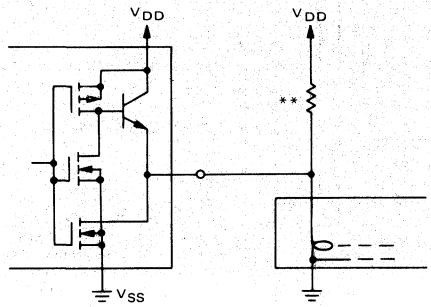
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

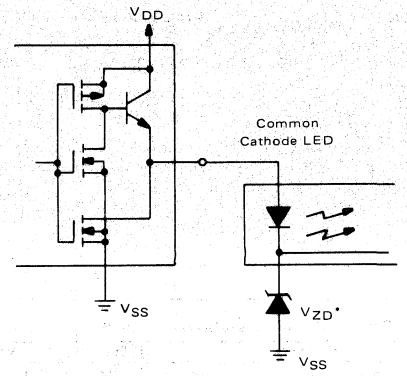




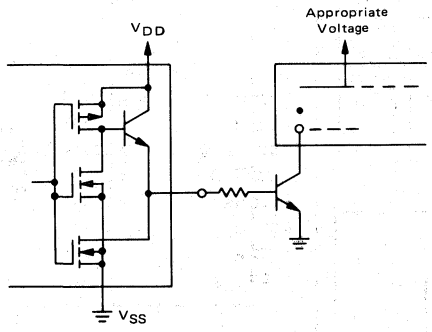
INCANDESCENT READOUT



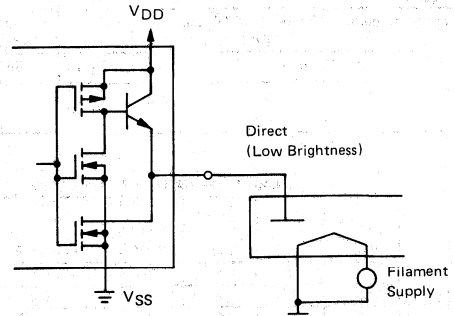
LIGHT-EMITTING DIODE (LED) READOUT USING A ZENER DIODE TO REPLACE DROPPING RESISTORS



GAS DISCHARGE READOUT



FLUORESCENT READOUT



V_{SS} or appropriate voltage below V_{SS}.

(Caution: Absolute maximum working voltage = 18.0 V)

* V_{ZD} should be set at $V_{DD} - 1.3\ V - V_{LED}$. Wattage of zener diode must be calculated for number of segments and worst-case conditions.

** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

MOTOROLA

MC14558B

BCD-TO-SEVEN SEGMENT DECODER

The MC14558B decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and $\overline{RBI}$, and provides an active-high seven-segment output for a display driver.

An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

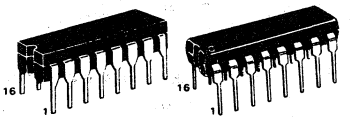
Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

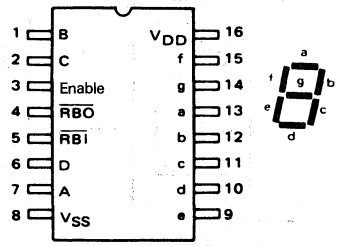
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Input Current, per Pin	I_{in}	±10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

AUXILIARY INPUT TRUTH TABLE

Enable Pin 3	$\overline{RBI}$ Pin 5	BCD Input Code	$\overline{RBO}$ Pin 4	Function Performed
0	0	X	0	Lamp Test
0	1	X	1	Blank Segments
1	1	0	1	Display Zero
1	0	0	0	Blank Segments
1	X	1-9	1	1-9 Displayed

X = Don't Care
$\overline{RBI}$ = Ripple Blanking Input
$\overline{RBO}$ = Ripple Blanking Output

PIN ASSIGNMENT



DISPLAY

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package) V_{in} = 0 or V_{DD}		10	–	10	–	0.010	10	–	300	
I_{out} = 0 μA		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package) V_{in} = 0 or V_{DD}		10	–	40	–	0.010	40	–	300	
I_{out} = 0 μA		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C; see Figure 1)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 495 ns		5.0	–	580	1160	
t_{PLH} = (0.66 ns/pF) C_L + 187 ns		10	–	220	440	
t_{PLH} = (0.5 ns/pF) C_L + 120 ns		15	–	145	230	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 695 ns		5.0	–	780	1560	
t_{PHL} = (0.66 ns/pF) C_L + 242 ns		10	–	275	550	
t_{PHL} = (0.5 ns/pF) C_L + 160 ns		15	–	185	370	

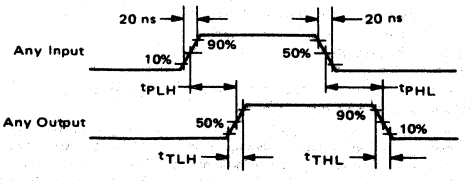
* The formulae given are for the typical characteristics only.

TRUTH TABLE

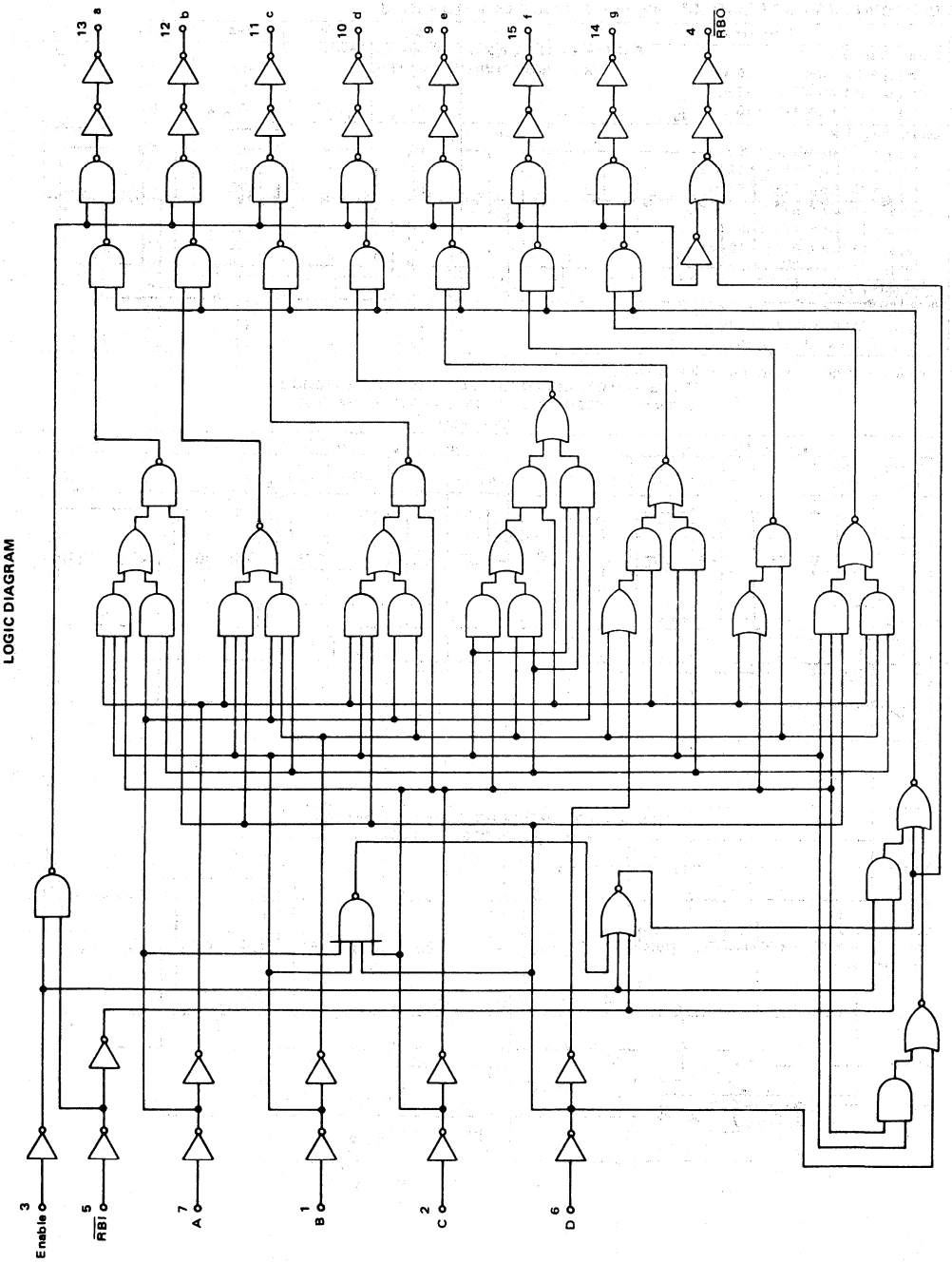
INPUTS						OUTPUTS*								
Enable Pin 3	$\overline{RBI}$ Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	$\overline{RBO}$ Pin 4	DISPLAY
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0
1	X	0	0	0	1	0	0	0	0	1	1	0	1	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1	2
1	X	0	0	1	1	1	1	1	1	0	0	1	1	3
1	X	0	1	0	0	0	1	1	0	0	1	1	1	4
1	X	0	1	0	1	1	0	1	1	0	1	1	1	5
1	X	0	1	1	0	0	0	1	1	1	1	1	1	6
1	X	0	1	1	1	1	1	1	0	0	0	0	1	7
1	X	1	0	0	0	1	1	1	1	1	1	1	1	8
1	X	1	0	0	1	1	1	1	0	0	1	1	1	9
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
0	0	X	X	X	X	1	1	1	1	1	1	1	0	8
0	1	X	X	X	X	0	0	0	0	0	0	0	1	Blank

*All non-valid BCD input codes produce a blank display.
X = Don't Care

FIGURE 1 – SIGNAL WAVEFORMS



LOGIC DIAGRAM



TYPICAL APPLICATIONS

FIGURE 2 – LEADING AND TRAILING ZERO SUPPRESSION WITH LAMP TEST

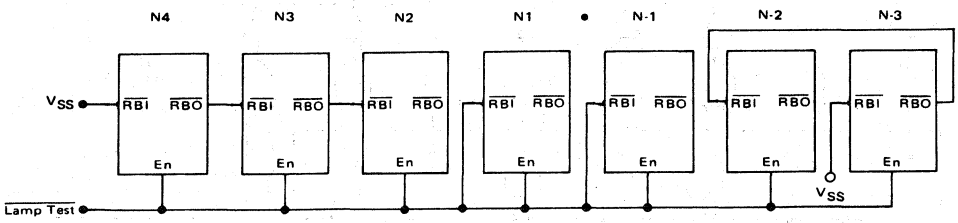


FIGURE 3 – LEADING AND TRAILING ZERO SUPPRESSION WITH PWM INTENSITY BLANKING AND NO LAMP TEST

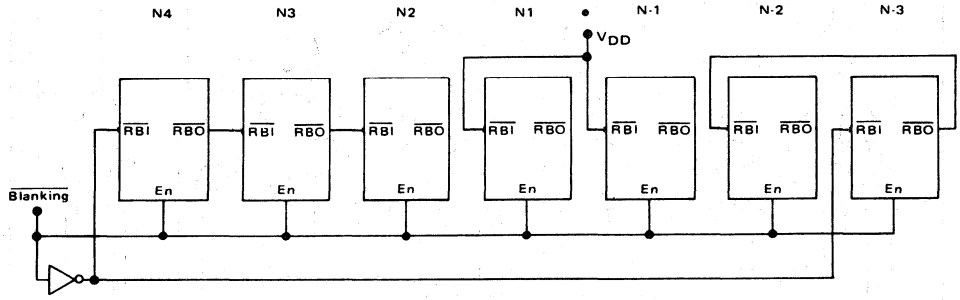
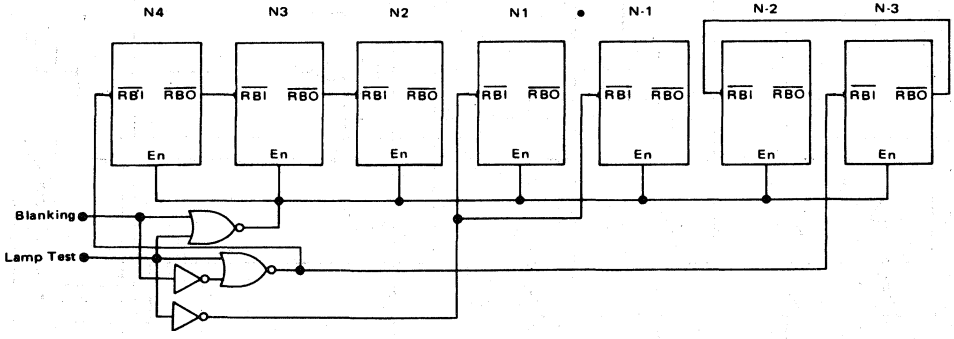


FIGURE 4 – ZERO SUPPRESSION WITH LAMP TEST AND INTENSITY BLANKING



MOTOROLA

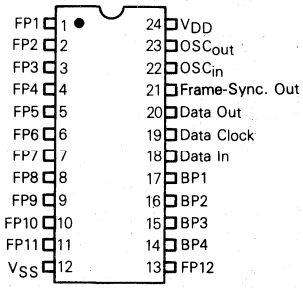
MC145000 < MC145001

SERIAL INPUT MULTIPLEXED LCD DRIVERS (MASTER AND SLAVE)

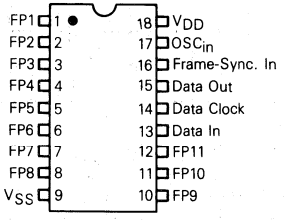
The MC145000 (Master) LCD Driver and the MC145001 (Slave) LCD Driver are CMOS devices designed to drive liquid crystal displays in a multiplexed-by-four configuration. The Master unit generates both frontplane and backplane waveforms, and is capable of independent operation. The Slave unit generates only frontplane waveforms, and is synchronized with the backplanes from the Master unit. Several Slave units may be cascaded from the Master unit to increase the number of LCD segments driven in the system. The maximum number of frontplanes is dependent upon the capacitive loading on the backplane drivers and the drive frequency. The devices use data from a microprocessor or other serial data and clock source to drive one LCD segment per bit.

- Direct Interface to CMOS Microprocessors
- Serial Data Port, Externally Clocked
- Multiplexing-By-Four
- Net dc Drive Component Less Than 50 mV
- Master Drives 48 LCD Segments
- Slave Provides Frontplane Drive for 44 LCD Segments
- Drives Large Segments—Up to one Square Centimeter
- Supply Voltage Range = 3 V to 6 V
- Latch Storage of Input Data
- Low Power Dissipation
- Logic Input Voltage Can Exceed V_{DD}
- Accomodates External Temperature Compensation
- See Application Note AN-823A, Section 4
- Chip Complexities: MC145000—1723 FETs or 431 Equivalent Gates
  MC145001—1495 FETs or 374 Equivalent Gates

PIN ASSIGNMENTS



MC145000
Master

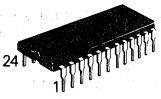


MC145001
Slave

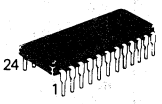
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT
MULTIPLEXED LCD DRIVERS
(MASTER AND SLAVE)

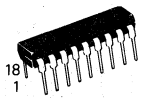


L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXX
- Suffix Denotes
  - L Ceramic Package
  - P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the ranges $V_{SS} \leq V_{out} \leq V_{DD}$ and $V_{SS} \leq V_{in} \leq 15$ V

Unused inputs must always be tied to an appropriate logic voltage level.

4

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +6.5	V
Input Voltage, Data In and Data Clock	V_{in}	−0.5 to 15	V
Input Voltage, Pin 22 of Master	$V_{in\ osc}$	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

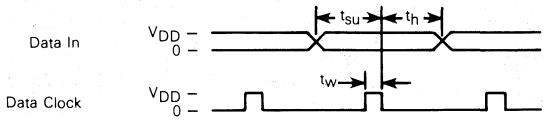
Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
RMS Voltage Across a Segment (BPi-FPj) "ON" Segment	V_{ON}	3.0	–	–	–	1.73	–	–	–	V
		6.0	–	–	–	3.46	–	–	–	
"OFF" Segment	V_{OFF}	3.0	–	–	–	1.00	–	–	–	V
		6.0	–	–	–	2.00	–	–	–	
Average DC Offset Voltage	Vdc	3.0	–	30	–	10	30	–	30	mV
		6.0	–	50	–	20	50	–	50	
Input Voltage "0" Level	V_{IL}	3.0	–	0.90	–	1.35	0.90	–	0.90	V
		6.0	–	1.80	–	2.70	1.80	–	1.80	
"1" Level	V_{IH}	3.0	2.10	–	2.10	1.65	–	2.10	–	V
		6.0	4.20	–	4.20	3.30	–	4.20	–	
Output Drive Current — Backplanes										
High-Current State*										
V_O = 2.85 V	I_{BH}	3.0	150	–	75	190	–	35	–	μA
V_O = 1.85 V			220	–	110	200	–	55	–	
V_O = 1.15 V			160	–	80	200	–	40	–	
V_O = 0.15 V			400	–	200	300	–	100	–	
V_O = 5.85 V	I_{BH}	6.0	500	–	250	300	–	125	–	μA
V_O = 3.85 V			1000	–	500	600	–	250	–	
V_O = 2.15 V			800	–	400	500	–	200	–	
V_O = 0.15 V			500	–	250	300	–	125	–	
Low-Current State*										
V_O = 2.85 V	I_{BL}	3.0	140	–	70	80	–	35	–	μA
V_O = 1.85 V			2.4	–	1.2	2.8	–	0.6	–	
V_O = 1.15 V			2.2	–	1.1	2.5	–	0.5	–	
V_O = 0.15 V			400	–	200	330	–	100	–	
V_O = 5.85 V	I_{BL}	6.0	190	–	95	105	–	45	–	μA
V_O = 3.85 V			15	–	7.5	10	–	3.7	–	
V_O = 2.15 V			13	–	6.5	9	–	3.2	–	
V_O = 0.15 V			850	–	425	570	–	210	–	
Output Drive Current — Frontplanes										
High-Current State*										
V_O = 2.85 V	I_{FH}	3.0	80	–	40	60	–	20	–	μA
V_O = 1.85 V			140	–	70	120	–	35	–	
V_O = 1.15 V			180	–	60	100	–	30	–	
V_O = 0.15 V			100	–	50	95	–	25	–	
V_O = 5.85 V	I_{FH}	6.0	140	–	70	90	–	35	–	μA
V_O = 3.85 V			360	–	180	250	–	90	–	
V_O = 2.15 V			400	–	200	240	–	100	–	
V_O = 0.15 V			100	–	50	120	–	25	–	
Low-Current State*										
V_O = 2.85 V	I_{FL}	3.0	60	–	30	40	–	15	–	μA
V_O = 1.85 V			2.8	–	1.4	2.8	–	0.7	–	
V_O = 1.15 V			2.2	–	1.1	2.5	–	0.5	–	
V_O = 0.15 V			100	–	50	100	–	25	–	
V_O = 5.85 V	I_{FL}	6.0	100	–	50	60	–	25	–	μA
V_O = 3.85 V			16	–	8.0	10	–	4.0	–	
V_O = 2.15 V			13	–	6.5	9	–	3.2	–	
V_O = 0.15 V			200	–	100	175	–	50	–	
Input Current	I_{in}	6.0	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	3.0	–	10	–	2.5	15	–	20	μA
		6.0	–	185	–	50	175	–	130	

*For a time ($t \cong 2.56$/osc. freq.) after the backplane or frontplane waveform changes to a new voltage level, the circuit is maintained in the high-current state to allow the load capacitances to charge quickly. Then the circuit is returned to the low-current state until the next voltage level change occurs.

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Data Clock Frequency	f_{cl}	3.0 6.0	– –	12.5 24	7.5 12.5	MHz
Rise and Fall Times – Data clock	t_r, t_f	3.0 6.0	– –	– –	125 10	µs
Setup Time Data In to Data Clock	t_{su}	3.0 6.0	48 16	– –	– –	ns
Hold Time Data In to Data Clock	t_h	3.0 6.0	−5 0	– –	– –	ns
Pulse Width Data Clock	t_w	3.0 6.0	65 40	– –	– –	ns

SWITCHING WAVEFORMS



DEVICE OPERATION

Figure 1 shows a block diagram of the Master unit. The unit is composed of two independent circuits: the data input circuit with its associated data clock, and the LCD drive circuit with its associated system clock.

Forty-eight bits of data are serially clocked into the shift register on the falling edges of the external data clock. Data in the shift register is latched into the 48-bit latch at the beginning of each frame period. (As shown in Figure 3, the frame period, t_{frame}, is the time during which all the LCD segments are set to the desired "ON" or "OFF" states.)

The binary data present in the latch determines the appropriate waveform signal to be generated by the frontplane drive circuits, whereas the backplane waveforms are invariant. The frontplane and backplane waveforms, FPn and BPn, are generated using the system clock (which is the oscillator divided by 256) and voltages from the V/3 generator circuit (which divides V_{DD} into one-third increments). As shown in Figure 3, the frontplane and backplane waveforms and the "ON" and "OFF" segment waveforms have periods equal to t_{frame} and frequencies equal to the system clock divided by four.

Twelve frontplane and four backplane drivers are available from the Master unit. The latching of the data at the beginning of each frame period and the carefully balanced voltage-generation circuitry minimize the generation of a net dc component across any LCD segment.

The Slave unit (Figure 2) consists of the same circuitry as the Master unit, with two exceptions: it has no backplane drive circuitry, and its shift register and latch hold 44 bits. Eleven frontplane and no backplane drivers are available from the Slave unit.

LCD DRIVER SYSTEM CONFIGURATIONS

Figure 4 shows a basic LCD Driver system configuration, with one Master and several Slave units. The maximum number of slave units in a system is dictated by the maximum backplane drive capability of the device and by the system data update rate. Data is serially shifted first into the Master unit and then into the following Slave units on the falling edge of the common data clock. The oscillator is common to the Master unit and each of the Slave units. At the beginning of each frame period, t_{frame}, the Master unit generates a frame-sync pulse (Figure 3) which is received by the Slave units. The pulse is to ensure that all Slave unit frontplane drive circuits are synchronized to the Master unit's backplane drive circuits.

A single multiplexed-by-four, 7-segment (plus decimal point) LCD and possible frontplane and backplane connections are shown in Figure 5. When several such displays are used in a system, the four backplanes generated by the Master unit are common to all the LCD digits in the system. The twelve frontplanes of the Master unit are capable of controlling forty-eight LCD segments (6 LCD digits), and the eleven frontplanes of each Slave unit are capable of controlling forty-four LCD segments (5½ LCD digits).

FIGURE 1 — BLOCK DIAGRAM OF THE MC145000 (MASTER) LCD DRIVER

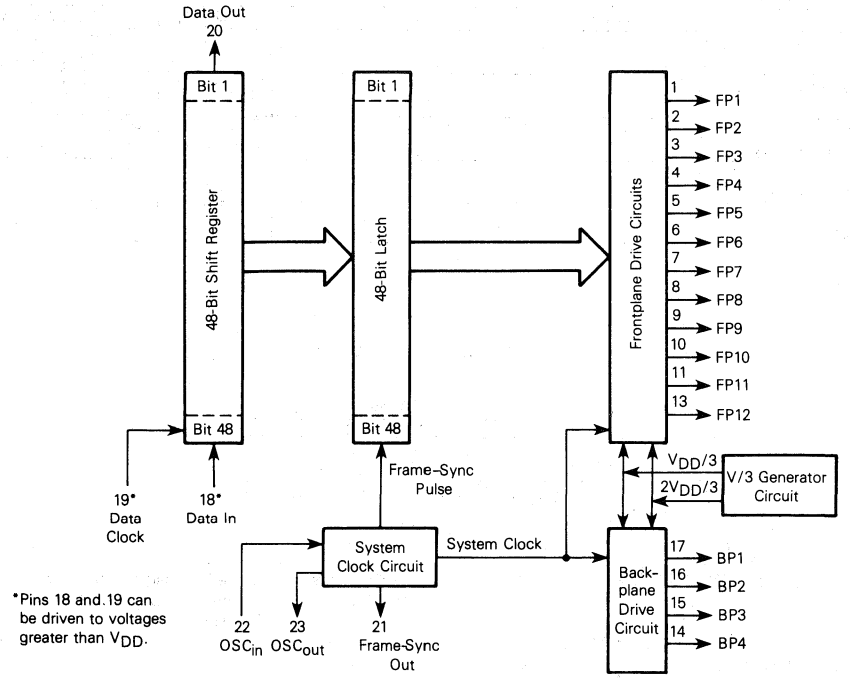


FIGURE 2 — BLOCK DIAGRAM OF THE MC145001 (SLAVE) LCD DRIVER

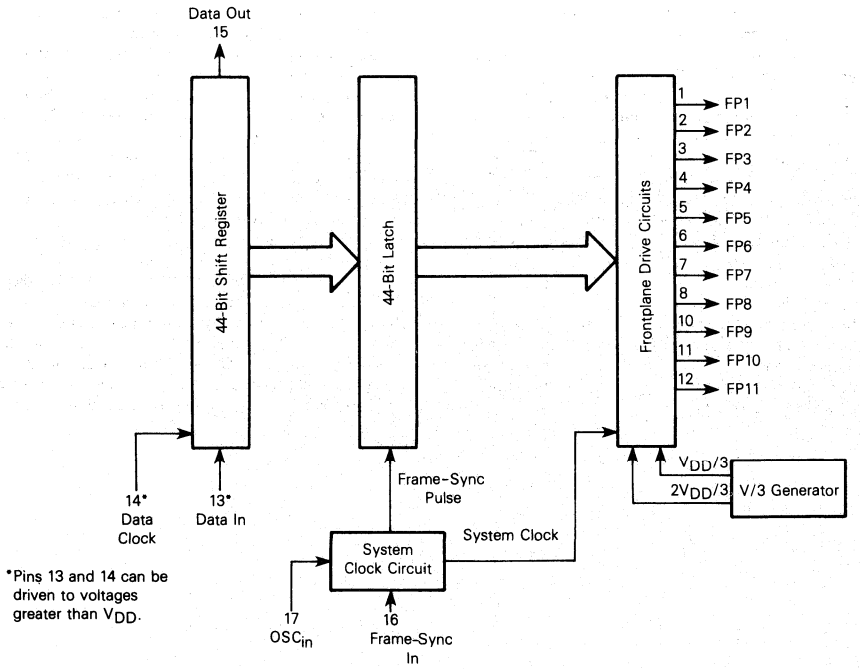


FIGURE 3 — VOLTAGE WAVEFORMS

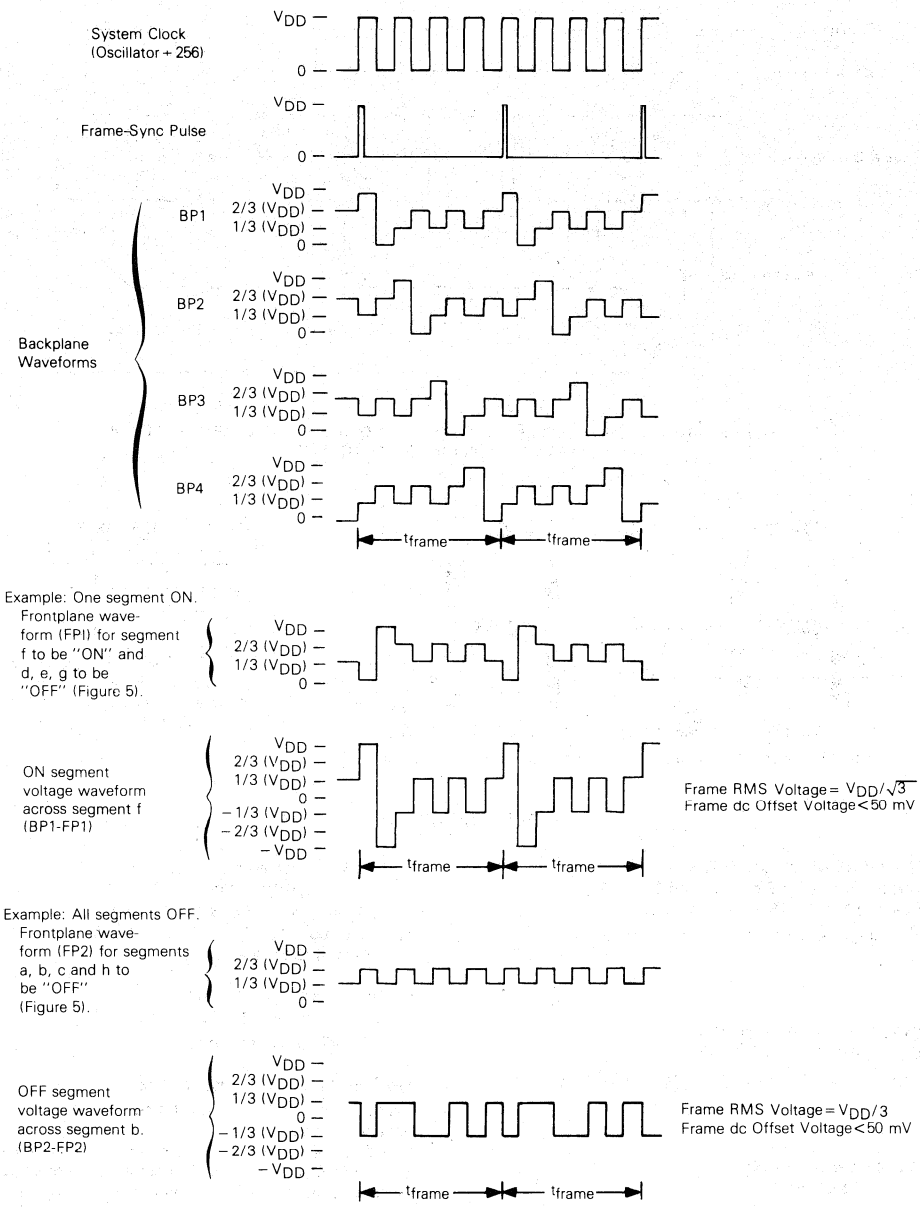


FIGURE 4 — BASIC SYSTEM CONFIGURATION

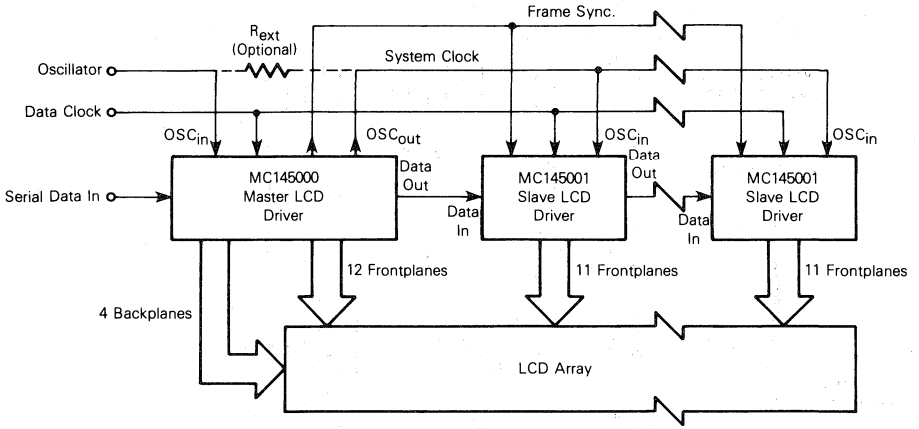
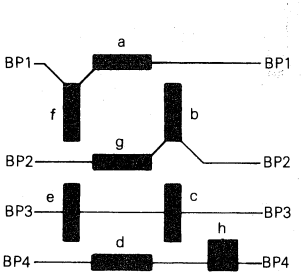
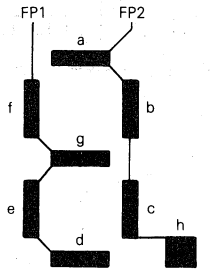


FIGURE 5 — FRONTPLANE AND BACKPLANE CONNECTIONS TO A MULTIPLEXED-BY-FOUR 7-SEGMENT (PLUS DECIMAL POINT) LCD



Typical Backplane Configuration



Typical Frontplane Configuration

SEGMENT TRUTH TABLE*

	FP1	FP2
BP1	f	a
BP2	g	b
BP3	e	c
BP4	d	d

*Because there is no standard for backplane and frontplane connections on multiplexed displays, this truth table may be used only for this example.

PIN DESCRIPTIONS

FRONTPLANE DRIVE OUTPUTS
(Master: FP1-FP12; Pins 1-11 and 13)
(Slave: FP1-FP11; Pins 1-8 and 10-12)

The frontplane drive waveforms for the LCDs.

BACKPLANE DRIVE OUTPUTS
(Master: BP1-BP4; Pins 14-17)

The backplane drive waveforms for the LCDs.

DATA IN (Master: Pin 18)
(Slave: Pin 13)

The serial data input pin. Data is clocked into the shift register on the falling edge of the data clock. A high logic level will cause the corresponding LCD segment to be turned on, and a low logic level will cause the segment to be turned off. This pin can be driven to 15 volts regardless of the value of V_{DD}, thus permitting optimum display drive voltage.

DATA CLOCK (Master: Pin 19)
(Slave: Pin 14)

The input pin for the external data clock, which controls the shift registers. This pin can be driven to 15 volts regardless of the value of V_{DD}.

DATA OUT (Master: Pin 20)
(Slave: Pin 15)

The serial data output pin.

FRAME-SYNC OUT (Master: Pin 21)

The output pin for the frame-sync pulse, which is generated by the Master unit at the beginning of each frame period, t_{frame}. From Figure 1, the 48-bit latch is loaded during the positive Frame-Sync Out pulse. Therefore, if the Data Clock is active during this load interval, the display will flicker.

FRAME-SYNC IN (Slave: Pin 16)

The input pin for the frame-sync pulse from the Master unit. The frame-sync pulse synchronizes the Slave frontplane drive waveforms to the Master backplane drive waveforms.

OSC_{in} (Master: Pin 22)
(Slave: Pin 17)

The input pin to the system clock circuit. The oscillator frequency is either obtained from an external oscillator or generated in the Master unit by connecting an external resistor between the OSC_{in} pin and the OSC_{out} pin (Pin 23). Figure 6 shows the relationship between resistor value and frequency.

OSC_{out} (Master: Pin 23)

The output pin of the system clock circuit. This pin is connected to the OSC_{in} input (Pin 17) of each Slave unit.

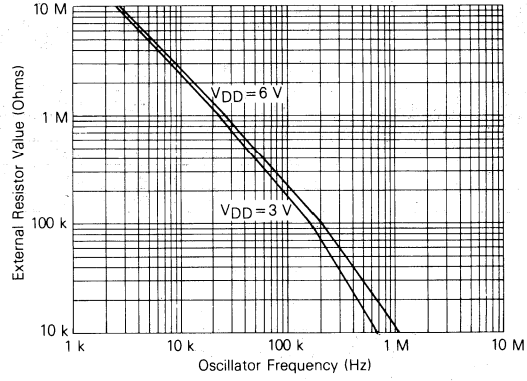
V_{DD} (Master: Pin 24)
(Slave: Pin 18)

The positive supply voltage.

V_{SS} (Master: Pin 12)
(Slave: Pin 9)

The negative supply (or ground) voltage.

FIGURE 6 — TYPICAL OSCILLATOR FREQUENCY vs EXTERNAL RESISTOR VALUE



4

APPLICATIONS

The following examples are presented to give the user further insight into the operation and organization of the Master and Slave LCD Drivers.

An LCD segment is turned either on or off depending upon the RMS value of the voltage across it. This voltage is equal to the backplane voltage waveform minus the frontplane voltage waveform. As previously stated, the backplane waveforms are invariant (see Figure 3). Figure 10 shows one period of every possible frontplane waveform.

For a detailed explanation of the operation of liquid crystal materials and multiplexed displays, refer to a brochure entitled "Multiplexed Liquid Crystal Displays," by Gregory A. Zaker, General Electric Company, Liquid XTAL Displays Operation, 24500 Highpoint Road, Cleveland, Ohio 44122.

Example 1: Many applications (e.g., meters, gasoline pumps, pinball machines, and automobile dashboard displays) require that, for each display update, an entirely new set of data must be shifted into the Master and cascaded Slave units. The correspondence between the frontplane-backplane intersections at the LCD segments and the data bit locations in the 48-bit latch of the Master (or 44-bit latch of the Slave) is necessary information to the system designer. In Figure 1, it is shown that data is serially shifted first into the 48th-bit location of the shift register of the Master. Thus, after 48 data bits have been shifted in, the first bit to be entered has been shifted into bit-location one, the second bit into bit-location two, and so on. Table 1 shows the bit location in the latch that controls the corresponding frontplane-backplane intersection. For example, the information stored in the 26th-bit location of the latch controls the LCD segment at the intersection of FP7 and BP3. The voltage waveform across that segment is equal to (BP3 minus FP7). The same table, but with the column for FP12 deleted, describes the operation of the Slave unit.

In applications of this type, all the necessary data to completely update the display are serially shifted into the Master and succeeding Slave units within a frame period. Typically, a microprocessor is used to accomplish this.

Example 2: Many keyboard-entry applications, such as calculators, require that the most significant digit be entered and displayed first. Then as each succeeding digit is entered, the previously entered digits must shift to the left. It is, therefore, neither necessary nor desirable to enter a completely new set of data for each display change. Figure 7 shows a representation of a system consisting of one Master and three Slave units and displaying 20 LCD digits. If each digit has the frontplane-backplane configuration shown in Figure 5, the relationship between frontplanes, backplanes, and LCD segments in the display is shown in Table 2.

Digits (or alphanumeric characters) are entered, most-significant digit first, by using a keyboard and a decoder external to the MC145000. Data is entered into the Master and cascaded Slave units according to the following format:

1) Initially, all registers and latches must be cleared by entering 160 zero data bits. This turns off all 160 segments of the display.

2) Entering the most-significant digit from the keyboard causes the appropriate eight bits to be serially shifted into the Master unit. These eight bits control LCD segments a through h of digit 1, and cause the desired digit to be displayed in the least-significant digit location.

3) Entering the second-most-significant digit from the keyboard causes eight more bits to be serially shifted into the Master unit. These eight bits now control LCD segments a through h of digit 1, and the previously entered eight bits now control segments a through h of digit 2. Thus the two digits are displayed in the proper locations.

4) Entering the remaining 18 digits from the keyboard fills the 20-digit display. Entering an extra digit will cause the first digit entered to be shifted off the display.

Example 3: In addition to controlling 7-segment (plus decimal point) digital displays, the MC145000 and MC145001 may be used to control displays using 5 × 7 dot matrices. A Master and three Slave units can drive 180 LCD segments, and therefore are capable of controlling five 5 × 7 dot matrices (175 segments). Two control schemes are presented in Figures 8 and 9; one using a single Master unit, and one using two Master units.

4

TABLE 1 — THE BIT LOCATIONS, IN THE LATCH, THAT CONTROL THE LCD SEGMENTS LOCATED AT EACH FRONTPLANE-BACKPLANE INTERSECTION

BACKPLANES	FRONTPLANES											
	FP1	FP2	FP3	FP4	FP5	FP6	FP7	FP8	FP9	FP10	FP11	FP12
BP1	4	8	12	16	20	24	28	32	36	40	44	48
BP2	3	7	11	15	19	23	27	31	35	39	43	47
BP3	2	6	10	14	18	22	26	30	34	38	42	46
BP4	1	5	9	13	17	21	25	29	33	37	41	45

FIGURE 7 — A 20-DIGIT DISPLAY (EQUIVALENT TO A 4 × 40 ARRAY)

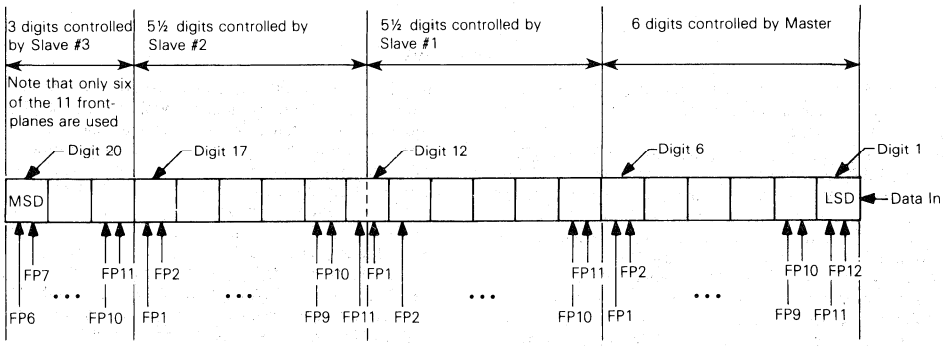


TABLE 2 — THE RELATIONSHIP BETWEEN FRONTPLANE-BACKPLANE INTERSECTIONS AND LCD SEGMENTS FOR THE SYSTEM CONFIGURATION OF FIGURE 7

	Master							Slave #1				Slave #2						Slave #3				
	FP12	FP11	FP10	FP9	• • •	FP2	FP1	FP11	FP10	• • •	FP1	FP11	FP10	FP9	• • •	FP2	FP1	FP11	FP10	• • •	FP7	FP6
BP1	a1	f1	a2	f2		a6	f6	a7	f7		a12	f12	a13	f13		a17	f17	a18	f18		a20	f20
BP2	b1	g1	b2	g2		b6	g6	b7	g7		b12	g12	b13	g13		b17	g17	b18	g18		b20	g20
BP3	c1	e1	c2	e2		c6	e6	c7	e7		c12	e12	c13	e13		c17	e17	c18	e18		c20	e20
BP4	h1	d1	h2	d2		h6	d6	h7	d7		h12	d12	h13	d13		h17	d17	h18	d18		h20	d20
	digit 1		digit 2		• • •	digit 6		digit 7		• • •	digit 12	digit 13			• • •	digit 17		digit 18		• • •	digit 20	

FIGURE 8 — EXAMPLE OF A 5×7 DOT MATRIX DISPLAY SYSTEM CONTROLLED BY ONE MASTER AND THREE SLAVE UNITS

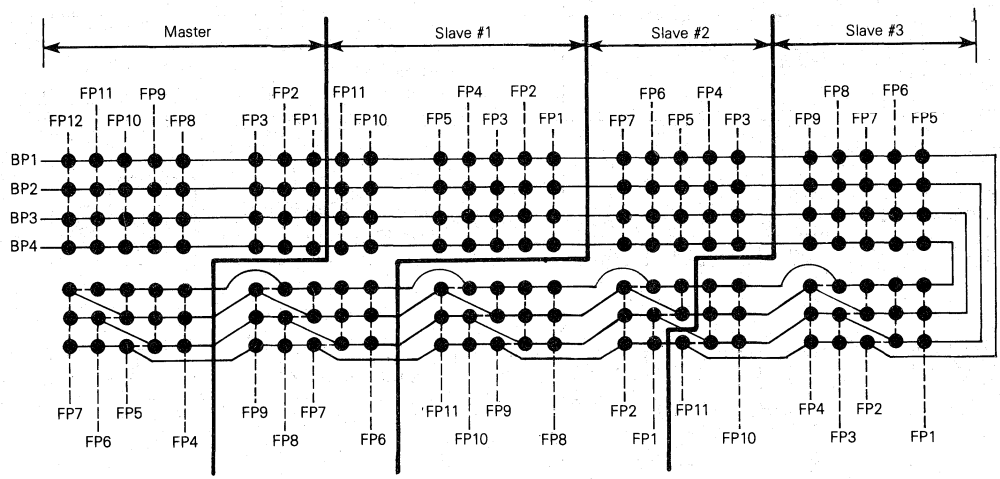
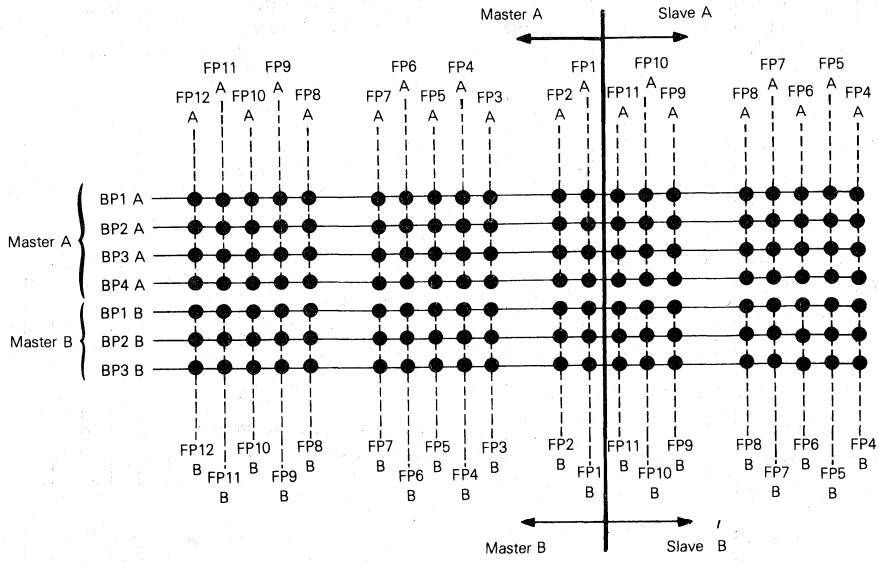
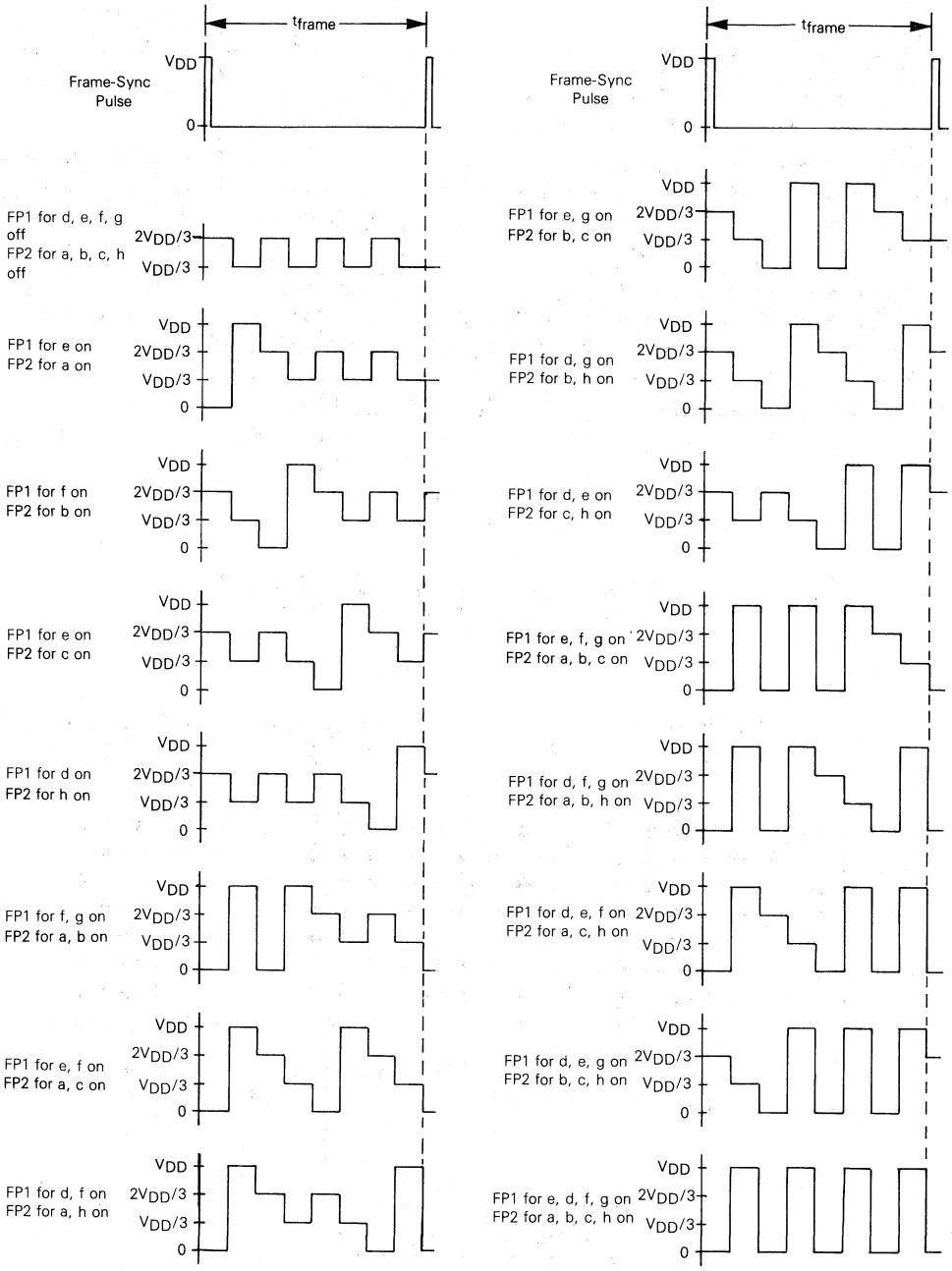


FIGURE 9 — EXAMPLE OF A 5×7 DOT MATRIX DISPLAY SYSTEM CONTROLLED BY TWO MASTER AND TWO SLAVE UNITS



LCDs can be obtained from:
AND, LXD, Hamlin, and other suppliers.

FIGURE 10 — POSSIBLE FRONTPLANE WAVEFORMS

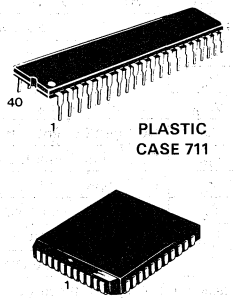


MOTOROLA

Advance Information

LCD Driver with Serial Interface

LSI CMOS



PLASTIC
CASE 711

PLASTIC LEADED
CHIP CARRIER (PLCC)
CASE 777

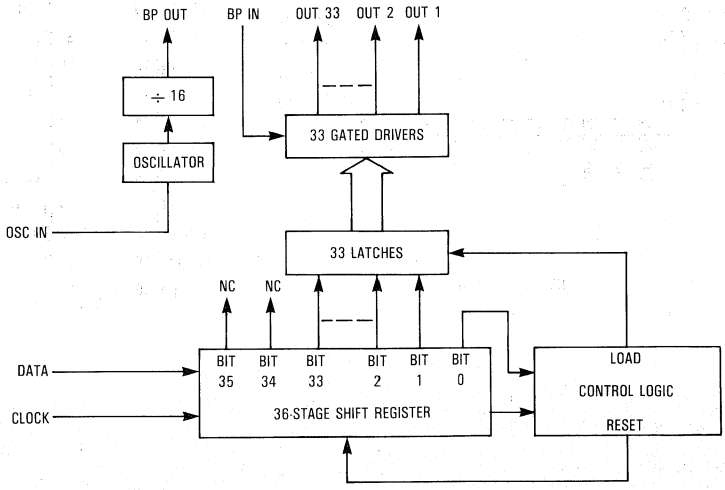
ORDERING INFORMATION
MC145453P Plastic DIP
MC145453FN PLCC

The MC145453 Liquid-Crystal Display Driver consists of a 36-stage serial-in/parallel-out shift register with 33 latches and drivers. Each package drives up to 33 non-multiplexed LCD segments; e.g., a 4½-digit, 7-segment-plus-decimal display. This device may be paralleled to increase the number of segments driven.

The input format is a Start Bit (high), followed by 33 Display Bits, plus 2 Trailing Bits (don't cares). A high Start Bit, after propagating to the last shift register stage, triggers generation of an internal load signal which transfers the 33 Display Bits into latches. An internal reset clears only the shift register which readies the device for the next bit stream.

- On-Chip Oscillator Provides 50 Percent Duty Cycle Backplane Drive
- No External Load Signal Required
- Operating Voltage Range: 3 to 10 V
- Operating Temperature Range: −40° to 85°C
- TTL-Compatible Inputs May Be Driven With CMOS
- May Be Used With Segmented-Alphanumeric, Bar-Graph, or Dot-Matrix LCDs
- Advantages Over Multiplexed LCD Systems: Wider Viewing Angle
  Optimum Contrast at Low Voltage
  Better Legibility at Extreme Temperature

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +11.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

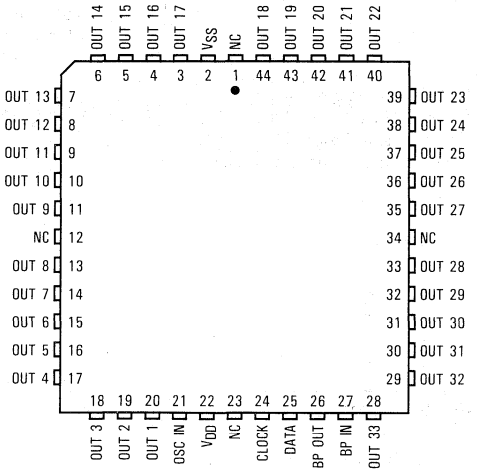
*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating: −12 mW/°C from 65°C to 85°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

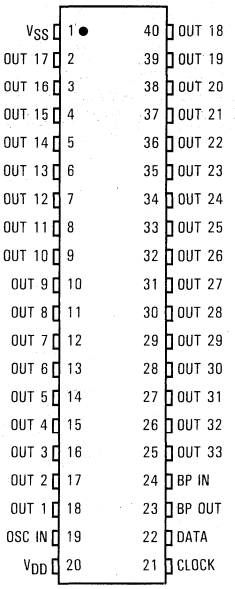
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD} except Osc In which must be tied to V_{SS}). Unused outputs must be left open.

4

PIN ASSIGNMENTS



NC = NO CONNECTION



Data sheet continued following page 11-9

CMOS Operational Amplifiers/Comparators

5

CMOS OPERATIONAL AMPLIFIERS/COMPARATORS

Device Number	Function
MC14573	Quad Programmable Op Amp
MC14574	Quad Programmable Comparator
MC14575	Programmable Dual Op Amp/Dual Comparator

Function	Quantity Per Package	Single Supply Voltage Range	Dual Supply Voltage Range	Frequency Range	Device Number	Number of Pins
Operational Amplifiers	4	3 to 15 V	±1.5 to ±7.5 V	DC to ~1 MHz	**MC14573**	16
Comparators	4	3 to 15 V	±1.5 to ±7.5 V	DC to ~1 MHz	**MC14574**	16
Operational Amplifiers and Comparators	2 and 2	3 to 15 V	±1.5 to ±7.5 V	DC to ~1 MHz	**MC14575**	16

MOTOROLA

MC14573
MC14574
MC14575

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER
QUAD PROGRAMMABLE COMPARATOR
DUAL/DUAL PROGRAMMABLE AMPLIFIER-COMPARATOR

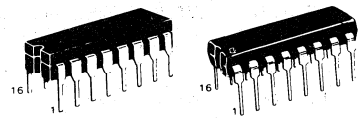
The MC14573, MC14574, and MC14575 are a family of quad operational low power amplifiers and comparators using the complementary P-channel and N-channel enhancement MOS devices in a single monolithic structure. The operating current is externally programmed with a resistor to provide a choice in the tradeoff of power dissipation and slew rates. The operational amplifiers are internally compensated.

These low cost units are excellent building blocks for consumer, industrial, automotive and instrument applications. Active filters, voltage reference, function generators, oscillators, limit set alarms, TTL-to-CMOS or CMOS-to-CMOS up converters, A-to-D converters and zero crossing detectors are some applications. These units are useful in both battery and line operated systems.

- Low Cost Quads
- Power Supply — Single 3.0 to 15 V
  Dual ±1.5 to ±7.5 V
- Wide Input Voltage Range
- Common Mode Range 0.0 to V_{DD} — 2.0 V for Single Supply
- Externally Programmable Power Consumption with One or Two Resistors
- Internally Compensated Operational Amplifiers
- High Input Impedance
- Comparators — JEDEC B-Series Compatible
- Chip Complexities: MC14573—30 FETs
  MC14574—38 FETs
  MC14575—46 FETs

CMOS MSI

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER
QUAD PROGRAMMABLE COMPARATOR
DUAL/DUAL PROGRAMMABLE OPERATIONAL AMPLIFIER-COMPARATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX

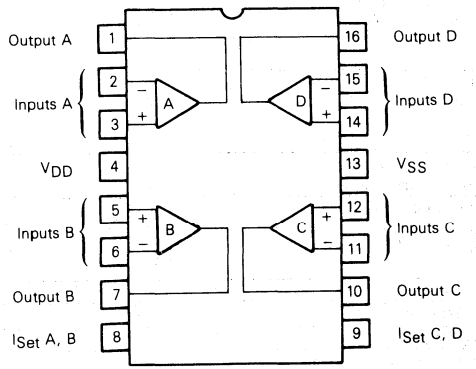
Suffix	Denotes
L	Ceramic Package
P	Plastic Package
C	Limited Operating Temperature Range

MC14573
Quad Op Amplifier

MC14574
Quad Comparator

MC14575
Dual Op Amplifier (A & B) plus Dual Comparator (C & D)

PIN ASSIGNMENT



MAXIMUM RATINGS† (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Programming Current Range	I_{Set}	2	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Package Power Dissipation*	P_D	800	mW

*Derate above 25°C @ 4.6 mW/°C
†Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$

RECOMMENDED OPERATING RANGE

Rating		Symbol	Value	Unit
DC Supply Voltage		V_{DD} to V_{SS}	+3.0 to +15	V
Programming Current	V_{DD} = 3 V 5 V < V_{DD} < 15 V	I_{Set}	2 to 50 2 to 750	μA

OPERATIONAL AMPLIFIER ELECTRICAL CHARACTERISTICS
(I_{Set} = 20 μA, R_L = 10 MΩ, C_L = 15 pF, T_A = 25°C, unless otherwise indicated)

Characteristic		Symbol	V_{DD} V	Min	Typ	Max	Unit
Input Common Mode Voltage Range		V_{ICR}	3 5 10 15	0 0 0 0	– – – –	1.5 3.5 8.5 13.5	V
Output Voltage Range R_L = 1 MΩ to V_{SS}		V_{OR}	3 5 10 15	0.05 0.05 0.05 0.05	– – – –	2.95 4.95 9.95 14.90	V
Input Offset Voltage MC14573, MC14575		V_{IO}	3 5 10 15	– – – –	±5 ±8 ±10 ±10	±30 ±30 ±30 ±30	mV
Average Temperature Coefficient of V_{IO}		$\Delta V_{IO}/\Delta T$	–	–	15	–	μV/°C
Input Capacitance		C_{in}	–	–	5	10	pF
Input Bias Current		I_{IB}	–	–	1	50	pA
Input Bias Current	T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current		I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain	V_O = 1 V p-p V_O = 3 V p-p V_O = 6 V p-p V_O = 9 V p-p	A_{VOL}	3 5 10 15	2 8 8 8	8 10 12 12	– – – –	V/mV
Power Supply Rejection Ratio MC14573, MC14575		PSRR	3 5 10 15	45 54 54 54	57 67 67 67	– – –	dB
Common Mode Rejection Ratio MC14573, MC14575		CMRR	3 5 10 15	45 50 54 54	70 73 75 75	– – – –	dB
Output Source Current V_{OH} = V_{DD} −0.6 V		I_{OH}	5	55	80	–	μA
Output Sink Current $V_{in}+ = V_{DD}/2+0.5$ $V_{in}- = V_{DD}/2-0.5$	V_{OL} = 0.4 V V_{OL} = 0.4 V V_{OL} = 0.5 V V_{OL} = 1.5 V	I_{OL}	3 5 10 15	2.1 2.5 5.5 15	4.2 5.0 11.0 30	– – – –	mA
Slew Rate		S_R	–	0.6	0.8	–	V/μs
Unity Gain Bandwidth		G_{BW}	5	0.5	1	–	MHz
Phase Margin		ϕM	–	–	45	–	Degrees
Channel Separation		–	–	–	80	–	dB
Supply Current, Per Pair	$R_L = \infty$, I_{Set} = 20 μA, V_{in+} = 1.0 V, V_{in-} = 0 V) ($R_L = \infty$, Pins 8 and 9 = V_{DD})	I_{DD}	5 15	– –	260 0.05	340 1.0	μA

OPERATIONAL AMPLIFIER ELECTRICAL CHARACTERISTICS

(I_{Set} = 200 μA, R_L = 10 MΩ, C_L = 15 pF, T_A = 25°C, unless otherwise indicated)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Input Common Mode Voltage Range	V_{ICR}	5	0	–	3	V
		10	0	–	8	
		15	0	–	13	
Output Voltage Range	V_{OR}	5	0.1	–	4.8	V
R_L = 100 k to V_{SS}		10	0.1	–	9.8	
		15	0.1	–	14.8	
Input Offset Voltage	V_{IO}	5	–	±8	±30	mV
MC14573, MC14575		10	–	±10	±30	
		15	–	±12	±30	
Average Temperature Coefficient of V_{IO}	$\Delta V_{IO}/\Delta T$	–	–	20	–	μV/°C
Input Capacitance	C_{in}	–	–	5	10	pF
Input Bias Current	I_{IB}	–	–	1	50	pA
Input Bias Current T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current	I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain V_O = 3 V p-p	A_{VOL}	5	1	2	–	V/mV
V_O = 6 V p-p		10	1	3	–	
V_O = 9 V p-p		15	1	4	–	
Power Supply Rejection Ratio	PSRR	5	45	54	–	dB
MC14573, MC14575		10	54	67	–	
		15	54	67	–	
Common Mode Rejection Ratio	CMRR	5	40	55	–	dB
MC14573, MC14575		10	50	67	–	
		15	50	70	–	
Output Source Current $V_{OH} = V_{DD} - 1.5$ V	I_{OH}	15	550	800	–	μA
Output Sink Current V_{OH} = 0.4 V	I_{OL}	5	2.2	4.2	–	mA
V_{OH} = 0.5 V		10	5.0	10.0	–	
V_{OH} = 1.5 V		15	15	30	–	
Slew Rate	S_R	–	5	7	–	V/μs
Unity Gain Bandwidth	G_{BW}	5	1.5	3	–	MHz
Phase Margin	ϕM	–	–	48	–	Degrees
Channel Separation	–	–	–	80	–	dB
Supply Current, Per Pair ($R_L = \infty$, V_{in+} = 1.0 V, V_{in-} = 0 V)	I_{DD}	15	–	2.6	3.4	mA

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COMPARATOR ELECTRICAL CHARACTERISTICS (I_{Set} = 20 µA, R_L = 10 MΩ, C_L = 50 pF, T_A = 25°C, unless otherwise indicated)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Input Common Mode Voltage Range	V_{ICR}	3	0	–	1.5	V
		5	0	–	3.5	
		10	0	–	8.5	
		15	0	–	13.5	
Output Voltage Range "0" Level	V_{OL}	3	–	0	0.05	V
		5	–	0	0.05	
		10	–	0	0.05	
		15	–	0	0.05	
Output Voltage Range "1" Level	V_{OH}	3	2.95	3	–	V
		5	4.95	5	–	
		10	9.95	10	–	
		15	14.95	15	–	
Input Offset Voltage MC14574, MC14575	V_{IO}	3	–	±8	±30	mV
		5	–	±8	±30	
		10	–	±10	±30	
		15	–	±10	±30	
Average Temperature Coefficient of V_{IO}	$\Delta V_{IO}/\Delta T$	–	–	15	–	µV/°C
Input Capacitance	C_{in}	–	–	5	10	pF
Input Bias Current	I_{IB}	–	–	1	50	pA
Input Bias Current T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current	I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain	V_{OL}	3	1	20	–	V/mV
		5	1	10	–	
		10	1	6	–	
		15	1	6	–	
Power Supply Rejection Ratio MC14574, MC14575	PSRR	3	45	57	–	dB
		5	54	67	–	
		10	54	67	–	
		15	54	67	–	
Common Mode Rejection Ratio MC14574, MC14575	CMRR	3	45	55	–	dB
		5	50	65	–	
		10	54	67	–	
		15	54	67	–	
Output Source Current V_{OH} = 2.6 V	I_{OH}	3	−0.35	−0.65	–	mA
V_{OH} = 2.5 V		5	−2.5	−5.0	–	
V_{OH} = 4.6 V		5	−0.60	−1.1	–	
V_{OH} = 9.5 V		10	−1.3	−2.5	–	
V_{OH} = 13.5 V		15	−5.0	−9.5	–	
Output Sink Current V_{OL} = 0.4 V	I_{OL}	3	1.3	2.6	–	mA
V_{OL} = 0.4 V		5	1.9	3.8	–	
V_{OL} = 0.5 V		10	3.5	6.5	–	
V_{OL} = 1.5 V		15	14	25	–	
Output Rise and Fall Time, 100 mV Overdrive	t_{TLH}, t_{THL}	3	–	140	250	ns
		5	–	100	180	
		10	–	120	200	
		15	–	140	250	
Propagation Delay Time, 5 mV Overdrive	t_d	3	–	15	30	µs
		5	–	10	20	
		10	–	12	24	
		15	–	15	30	
Propagation Delay Time, 100 mV Overdrive	t_d	3	–	4	8	µs
		5	–	2	4	
		10	–	3	6	
		15	–	4	8	
Channel Separation	–	–	–	80	–	dB
Supply Current, Per Pair (R_L = ∞, I_{Set} = 20 µA, V_{in+} = 1.0 V, V_{in-} = 0 V)	I_{DD}	5	–	180	250	µA
(R_L = ∞, Pins 8 and 9 = V_{DD})		15	–	0.05	1.0	

COMPARATOR ELECTRICAL CHARACTERISTICS (I_{Set} = 200 µA, R_L = 10 MΩ, C_L = 50 pF, T_A = 25°C, unless otherwise indicated)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Input Common Mode Voltage Range	V_{ICR}	5	0	–	3	V
		10	0	–	8	
		15	0	–	13	
Output Voltage Range "0" Level	V_{OL}	5	–	0	0.05	V
		10	–	0	0.05	
		15	–	0	0.05	
Output Voltage Range "1" Level	V_{OH}	5	4.95	5	–	V
		10	9.95	10	–	
		15	14.95	15	–	
Input Offset Voltage MC14574, MC14575	V_{IO}	5	–	± 10	± 30	mV
		10	–	± 13	± 30	
		15	–	± 15	± 30	
Average Temperature Coefficient of V_{IO} T_A = −40°C to +85°C	$\Delta V_{IO}/\Delta T$	–	–	20	–	µV/°C
Input Capacitance	C_{in}	–	–	5	10	pF
Input Bias Current	I_{FB}	–	–	1	50	pA
Input Bias Current T_A = −40°C to +85°C	I_{IB}	–	–	–	1	nA
Input Offset Current	I_{IO}	–	–	–	100	pA
Open Loop Voltage Gain	A_{VOL}	5	2	7	–	V/mV
		10	1	4	–	
		15	1	4	–	
Power Supply Rejection Ratio MC14574, MC14575	PSRR	5	45	67	–	dB
		10	54	67	–	
		15	54	67	–	
Common Mode Rejection Ratio MC14574, MC14575	CMRR	5	40	65	–	dB
		10	50	67	–	
		15	50	67	–	
Output Source Current V_{OH} = 2.5 V	I_{OH}	3	−2.5	−5.0	–	mA
V_{OH} = 4.6 V		5	−0.60	−1.1	–	
V_{OH} = 9.5 V		10	−1.3	−2.5	–	
V_{OH} = 13.5 V		15	−5.0	−9.5	–	
Output Sink Current V_{OL} = 0.4 V	I_{OL}	5	1.9	3.8	–	mA
V_{OL} = 0.5 V		10	3.5	6.5	–	
V_{OL} = 1.5 V		15	14	25	–	
Output Rise and Fall Time, 100 mV Overdrive	t_{TLH}, t_{THL}	5	–	75	150	ns
		10	–	50	100	
		15	–	45	90	
Propagation Delay Time, 5 mV Overdrive	t_d	5	–	2.5	5.0	µs
		10	–	3.5	7	
		15	–	5	10	
Propagation Delay Time, 100 mV Overdrive	t_d	5	–	0.6	1.2	µs
		10	–	0.75	1.5	
		15	–	0.75	1.5	
Channel Separation	–	–	–	80	–	dB
Supply Current, Per Pair (R_L = ∞, V_{in+} = 1.0 V, V_{in-} = 0 V)	I_{DD}	15	–	1.8	2.5	mA

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The programming current I_{Set} is fixed by an external resistor R_{Set} connected between V_{SS} and either one or both of the I_{Set} pins (8 and 9). When two external programming resistors are used, the set currents for each op amp pair or comparator are given by:

$$I_{Set}\ (\mu A) \approx \frac{V_{DD} - V_{SS} - 1.5}{R_{Set}\ (M\Omega)}$$

Pins 8 and 9 may be tied together for use with a single programming resistor. The set currents for each op amp pair or comparator pair are then given by:

$$I_{Set\ A,\ B} = I_{Set\ C,\ D}\ (\mu A) \approx \frac{V_{DD} - V_{SS} - 1.5}{2\ R_{Set}\ (M\Omega)}$$

The total device current is typically 13 times I_{Set} per pair if the outputs are in the low state, and 5 times I_{Set} per pair if the outputs are in the high state. For op amps with an output in the linear region the device current will be between the values of 5 times and 13 times I_{Set}.

If a pair of op amps is not used, the I_{Set} pin for that pair may be tied to V_{DD} for minimum power consumption. To minimize power consumption in an unused pair of comparators this is not effective. The comparators should use a high value set resistor and the inputs should be set to a voltage that will force the output to V_{DD} (i.e., + in = V_{DD}, − in = V_{SS}).

It should be noted that increasing I_{Set} for comparators will decrease propagation delay for that comparator.

For operational amplifiers, the maximum obtainable output voltage (V_{OH}) for a given load resistor connected to V_{SS} is given by:

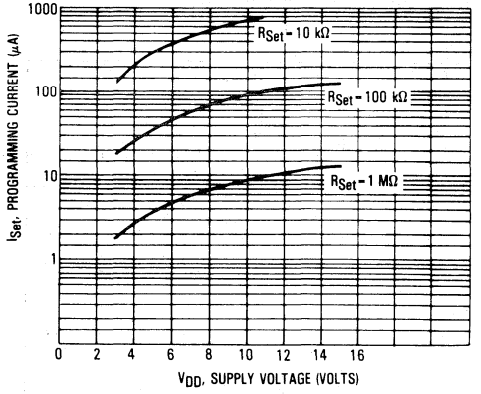
$$V_{OH} = 4 \times I_{Set} \times R_L - 0.05\ V,\ R_L \text{ in } \Omega,\ I_{Set} \text{ in A}$$

Note: V_{OH} Max = V_{DD}

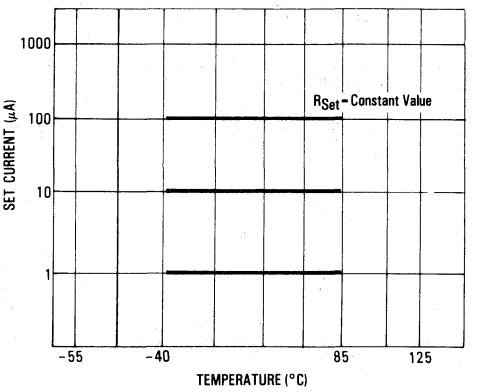
Typical op amp slew rates are given by:

$$S_R \approx 0.04\ I_{Set}\ (V/\mu s),\ I_{Set} \text{ in } \mu A$$

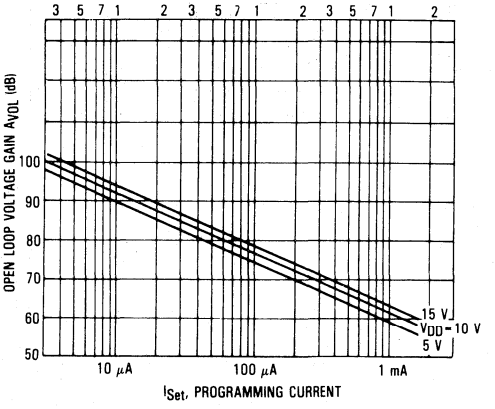
SET CURRENT versus V_{DD}



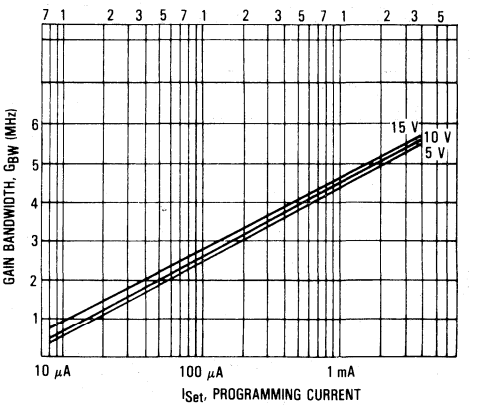
SET CURRENT versus TEMPERATURE



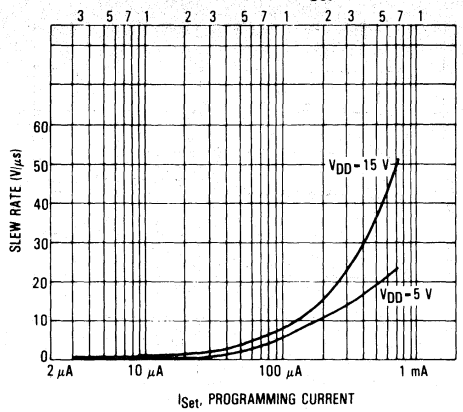
LOW FREQUENCY OPEN LOOP VOLTAGE GAIN versus I_{Set}



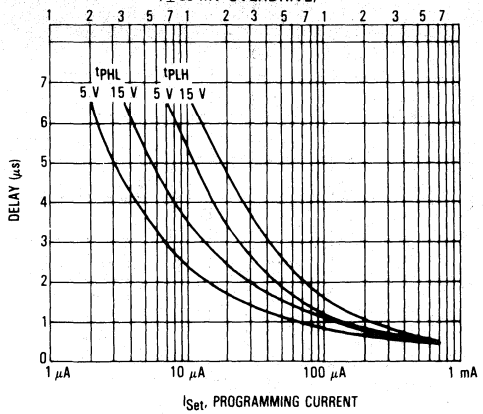
GAIN-BANDWIDTH PRODUCT versus I_{Set}



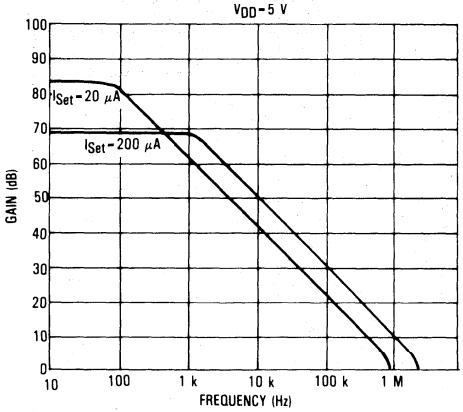
SLEW RATE versus I_{Set}



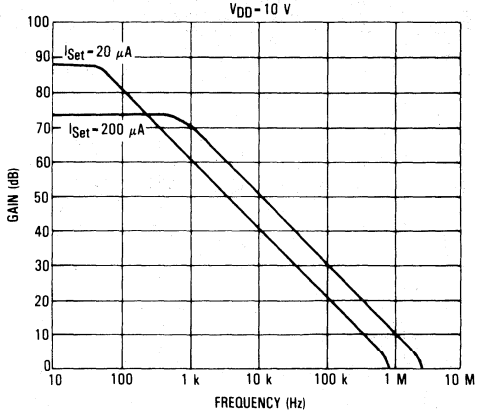
COMPARATOR PROPAGATION DELAY versus I_{Set}
(±50 mV OVERDRIVE)



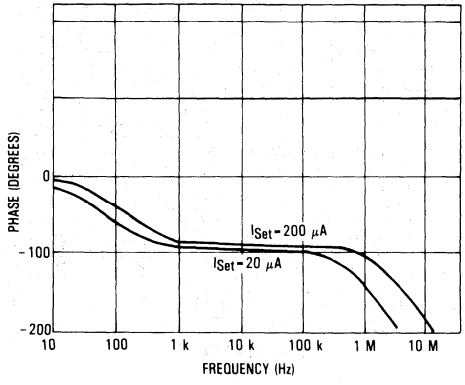
OPEN LOOP GAIN versus FREQUENCY
V_{DD} = 5 V



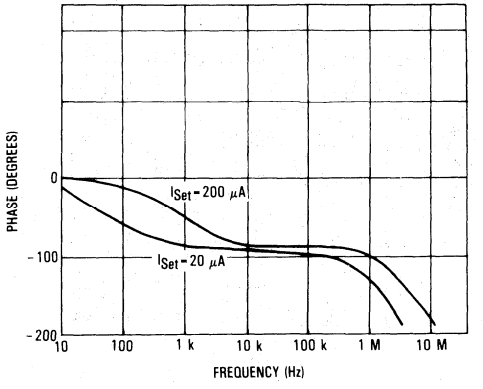
OPEN LOOP GAIN versus FREQUENCY
V_{DD} = 10 V



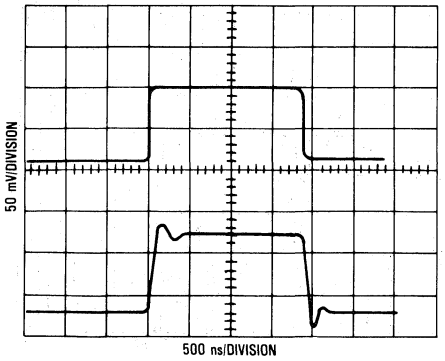
OPEN LOOP PHASE DELAY versus FREQUENCY
V_{DD} = 5 V



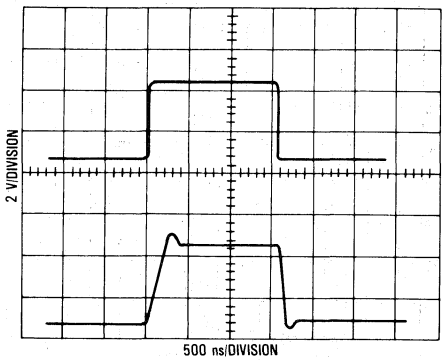
OPEN LOOP PHASE DELAY versus FREQUENCY
V_{DD} = 10 V



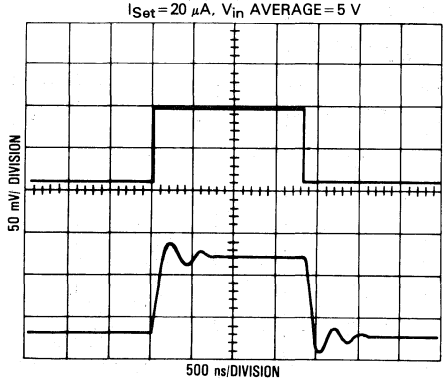
SMALL SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 200 μA, V_{in} AVERAGE = 5 V



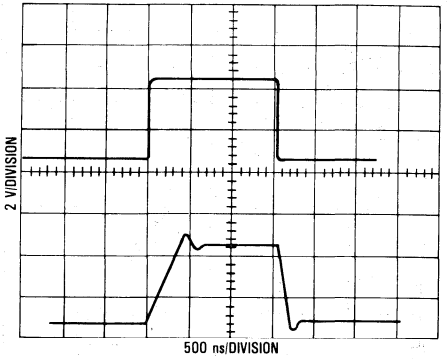
LARGE SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 200 μA, V_{in} AVERAGE = 5 V



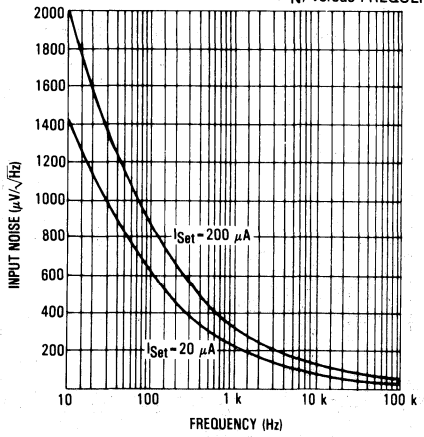
SMALL SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 20 μA, V_{in} AVERAGE = 5 V



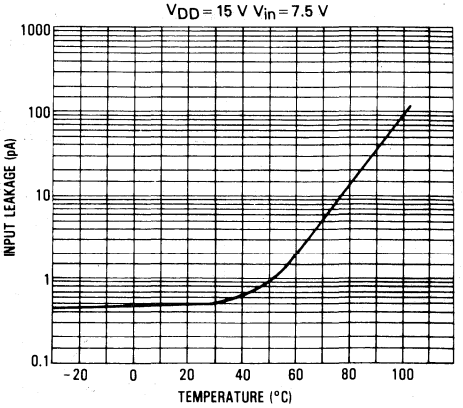
LARGE SIGNAL TRANSIENT RESPONSE
V_{DD} = 10 V NON-INVERTING UNITY GAIN
I_{Set} = 20 μA, V_{in} AVERAGE = 5 V



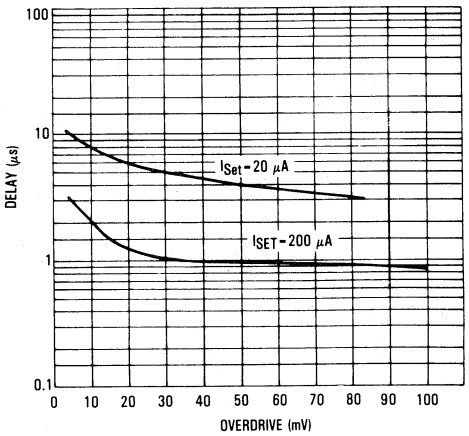
EQUIVALENT INPUT NOISE VOLTAGE (E_N) versus FREQUENCY



TYPICAL INPUT LEAKAGE versus TEMPERATURE
V_{DD} = 15 V V_{in} = 7.5 V

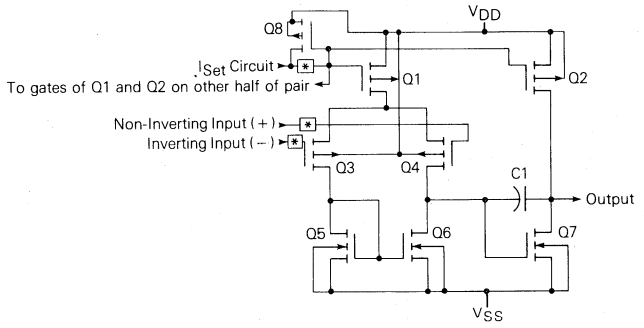


COMPARATOR PROPAGATION DELAY versus OVERDRIVE*
V_{DD} = 10 V, t_{PLH} and t_{PHL}

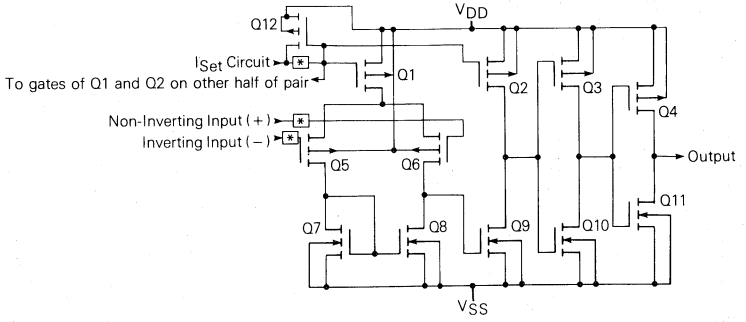


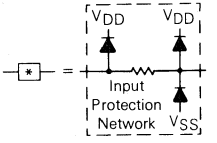
*A 10 mV overdrive is a signal on one input of a comparator that ranges from 10 mV less than the other input to 10 mV more than the other input.

OPERATIONAL AMPLIFIER SCHEMATIC
¼th CIRCUIT



COMPARATOR SCHEMATIC
¼th CIRCUIT





CMOS/NMOS PLLs/Frequency Synthesizers

6

Device Number	Function
MC6195*	Frequency Synthesizer TV Tuning System
MC6196*	Frequency Synthesizer TV Tuning System
MC14046B	Phase-Locked Loop
MC14568B	Phase Comparator and Programmable Counters
MC145106†	PLL Frequency Synthesizer
MC145145-1#	4-Bit Data Bus Input PLL Frequency Synthesizer
MC145146-1	4-Bit Data Bus Input PLL Frequency Synthesizer
MC145151-1	Parallel Input PLL Frequency Synthesizer
MC145152-1	Parallel Input PLL Frequency Synthesizer
MC145155-1	Serial Input PLL Frequency Synthesizer
MC145156-1	Serial Input PLL Frequency Synthesizer
MC145157-1	Serial Input PLL Frequency Synthesizer
MC145158-1	Serial Input PLL Frequency Synthesizer
MC145159-1	Serial Input PLL Frequency Synthesizer with Analog Phase Detector

*Closest equivalent for MC6190 through MC6194, which are being phased out and are not recommended for new designs.

†Closest equivalent for MC145104, MC145107, MC145109, MC145112, and MC145143, which are being phased out and are not recommended for new designs.

#Closest equivalent for MC145144, which is being phased out and is not recommended for new designs.

6

Divider Programming Format	Prescale Modulus	Single-Ended 3-State Phase Detector Output	Double-Ended Phase Detector Output	Number of Divider Stages ÷ R	÷ A	÷ N	Device Number	Number of Pins
Serial [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	Single	✓	✓	12*		14	MC145155-1	18
		✓	✓	14		14	MC145157-1	16
	Dual	✓	✓	12*	7	10	MC145156-1	20
		✓	✓	14	7	10	MC145158-1	16
		(Analog Detector Output)		14	7	10	MC145159-1	20
Parallel	Single	✓		11*		9	MC145106	18
		✓	✓	12*		14	MC145151-1	28
	Dual		✓	12*	6	10	MC145152-1	28
		✓			8*	4	MC14568B	16
4-Bit Bus	Single	✓	✓	12		14	MC145145-1	18
	Dual	✓	✓	12	7	10	MC145146-1	20
2 Control Lines	Single	✓		12★		12*	MC6195	20
		✓		12★		12*	MC6196	20
		✓					MC14046B	16

*Limited number of selectable values
★Mask-programmable to one fixed value

MOTOROLA

MC6190 MC6192
MC6191 MC6193
MC6194

FREQUENCY SYNTHESIZER TV TUNING SYSTEM

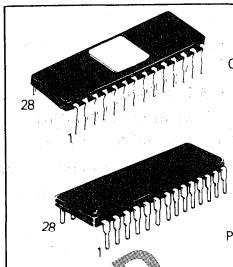
This series of phase locked loop subsystems is constructed in NMOS Silicon gate technology and are primarily intended for TV and CATV tuning applications. These products make it possible to receive all VHF and UHF TV frequencies.

- Single 5 V Supply
- Low External Parts Count
- Keyboard Interface Uses Low Cost 4 × 4 Keyboard
- Remote Control Capability
- Manual Channel Selection
- Scan Up/Scan Down
- Auto Programming of all Active Channels
- Automatic Switching to AFT Mode Option
- Channel Information Output Interfaces to Leds
- On Chip Reference Oscillator Uses External Crystal

MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

FREQUENCY SYNTHESIZER TV TUNING SYSTEM



L SUFFIX
CERAMIC PACKAGE
CASE 695

P SUFFIX
PLASTIC PACKAGE
CASE 710

NOT RECOMMENDED FOR NEW DESIGNS
PRODUCT BEING PHASED OUT

Closest equivalents are the MC6195 and MC6196

6

MOTOROLA

MC6195
MC6196

MOS
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

FREQUENCY SYNTHESIZER TV TUNING SYSTEM

FREQUENCY SYNTHESIZER TV TUNING SYSTEM

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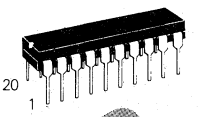
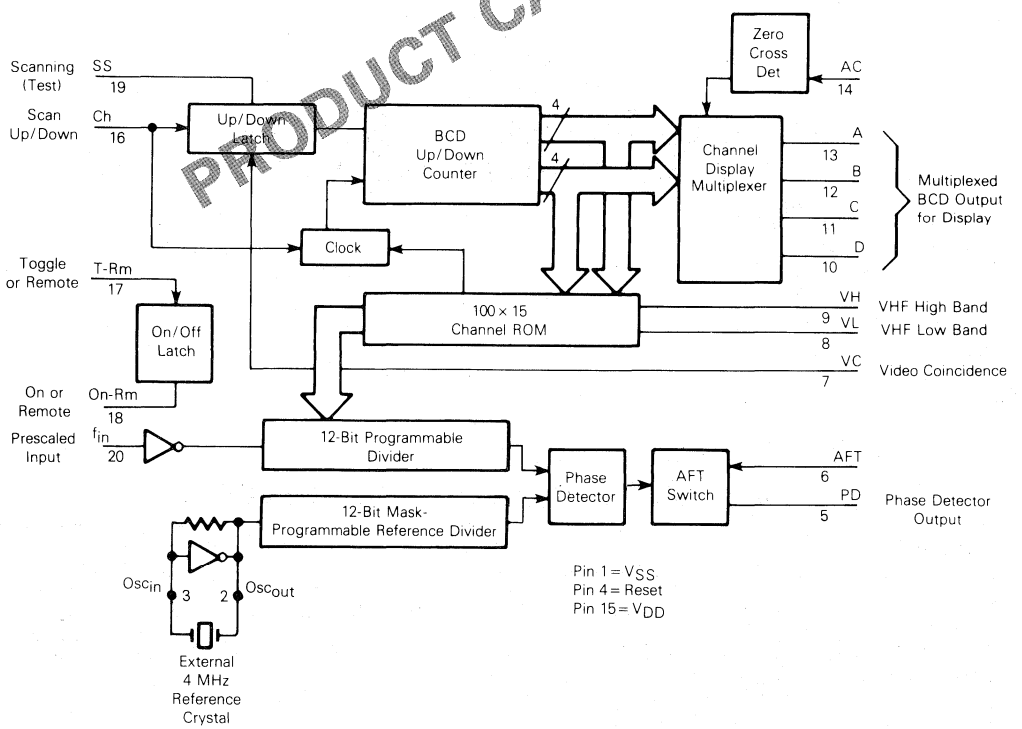


P SUFFIX
PLASTIC PACKAGE
CASE 738

BLOCK DIAGRAM



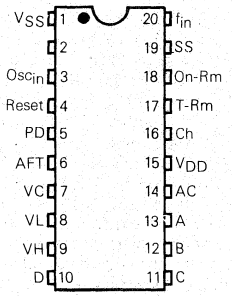
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage, All Inputs	V_{in}	−0.3 to +7	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−65 to +160	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, Voltages Referenced to V_{SS})

Characteristic			Symbol	V_{DD}	Min	Typ	Max	Units
Power Supply Voltage			V_{DD}	–	4.75	5.0	5.25	V
Output Voltage:								V
A, B, C, D,		0 Level	V_{OL}	5	–	–	0.8	
AFT		1 Level	V_{OH}	5	2.4	–	–	
Input Voltage:								V
	Reset, VC	0 Level	V_{IL}	5	–	–	0.8	
	On-Rm AFT (PLL Mode)	1 Level	V_{IH}	5	2.0	–	–	
	Ch, T-Rm	0 Level	V_{IL}	5	–	–	0.4	
		1 Level	V_{IH}	5	4.0	–	–	
Input Current:			I_{in}					μA
	f_{in}, Osc_{in}	$V_{IL}=0$ V, $V_{IH}=V_{DD}$		5	–	–	±20	
	Reset, VC	$V_{IL}=0$ V, $V_{IH}=V_{DD}$		5	–	–	±1	
	AC	$V_{AC}=V_{DD}$		5	–	–	300	
	AFT (PLL Mode)	$V_{IL}=0$ V		5	30	60	200	
	Ch, T-Rm	$V_{IL}=0$ V, $V_{IH}=4$ V		5	–	–	±200	
	A, B, C, D	$V_{IH}=V_{DD}$	I_{IH}	5	1.0	–	–	
		$V_{IL}=0$ V	I_{IL}	5	–	–	−3	mA
Input Capacitance			C_{in}	5	–	5	10	pF
Output Capacitance			C_{out}	5	–	6	10	pF
Output Current:			I_{OH}					μA
PD		$V_{OH}=1.2$ V		5	50	–	–	
A, B, C, D		$V_{OH}=2.7$ V		5	20	–	–	
A, B, C, D, VL, VH		$V_{OL}=0.4$ V	I_{OL}	5	400	–	–	
PD		$V_{OL}=1.2$ V		5	50	–	–	
On-Rm, SS		$V_{OL}=0.4$ V		5	1.6	–	–	mA
Output Leakage Current VL, VH, On-Rm, SS			I_L	5	–	–	10	μA
Output Leakage Current PD			I_L	5	–	–	±1	μA
Breakdown Voltage VL, VH, On-Rm, SS			V_{BDSO}	5	7	–	–	V
Quiescent Current, All Outputs Open			I_{DD}	5	–	–	60	mA

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF, $V_{DD} = 5$ V)

Characteristic		Symbol	Min	Typ	Max	Units
Output Rise Time		t_{TLH}	–	–	10	μs
Output Fall Time		t_{THL}	–	–	1	μs
Propagation Delay, AC to A, B, C, D (Outputs)		t_{PLH}, t_{PHL}	–	–	100	μs
Input Rise and Fall Times		t_{TLH}, t_{THL}	–	–	100	μs
Operating Frequency						MHz
f_{in}, Osc_{in}	$V_{in}=500$ mV p-p		–	8	4.1	
AC	$V_{in}=5$ V p-p		–	60	–	Hz

MC6190 FAMILY DEVICE CHARACTERISTICS

The Phase-Locked Loop Frequency Synthesizers MC6190 through MC6196 are products designed for use in various types of TV and CATV applications.

The MC6190 through MC6194 offer keyboard interface, BCD output data for channel display, band-switching information, AFT control, On/Off control, and battery or capacitor backup memory retention. The differences between these parts primarily have to do with the frequency divide numbers required for selected channels.

The MC6195 and MC6196 differ from the MC6190 through MC6194 in that they do not allow keyboard interface and do not have backup memory retention.

Some of the characteristics and intended applications are shown in the following table.

Device	Ref	Prescaler		Band	Lowest Channel	Highest Channel
		VHF	UHF			
MC6190	4 MHz	256	256	CATV	00	99
MC6191	4 MHz	256	256	USA	02	83
MC6192	4 MHz	256	256	Japan	01	62
MC6193	4 MHz	64	256	CATV	02	59
MC6194	3 MHz	64	256	CATV	02	60
MC6195	4 MHz	256	256	CATV	00	59
MC6196	4 MHz	256	256	USA	02	83

6

CIRCUIT OPERATION

The MC6195 and MC6196 are phase-locked loop frequency synthesizer devices that are the nucleus of digital tuning systems for CATV and USA TV converters. As shown in Figure 4 and 5, the devices interface with a linear control chip, an ECL prescaler, LED display interfacing devices, and a minimum of external components. The following sections will explain the functions of the various blocks in the block diagram.

ON/OFF OPERATION

ON/OFF LATCH – The On/Off Latch stores the On/Off information that is either directly received at T-Rm (Pin 17) or received from a remote source at On-Rm (pin 18).

If On/Off information is to be directly received at T-Rm, the latch operates as follows: When T-Rm is taken to V_{SS} (the direct-control mode) for at least two clock cycles (at AC, pin 14), the state of the On/Off Latch changes either from ON to OFF or from OFF to ON. In this mode of operation, On-Rm is the three-state output of the On/Off latch, and assumes the high-impedance state when the latch is toggled ON or the low-voltage level (V_{SS}) when the latch is toggled OFF.

If On/Off information is to be received at On-Rm from a remote source, the latch operates as follows: When T-Rm is taken to V_{DD} (the remote-control mode), On-Rm becomes the input from the remote-control unit. When taken to V_{DD}, On-Rm sets the On/Off Latch to the ON state. When taken to V_{SS}, On-Rm sets the latch to the OFF state.

The relationship between T-Rm, On-Rm, and the state of the On/Off Latch are illustrated in the flowchart in Figure 1.

CHANNEL-SCAN OPERATION

UP/DOWN LATCH – The Up/Down Latch stores the channel-scan information that is received at Ch (pin 16), and controls the direction of count of the BCD Up/Down Counter. The operation of the channel-scan circuitry is shown in the following table:

Input Voltage Level (Ch)	Channel-Scan Direction
Low ($\leq$0.4 V)	Down
High ($\geq$4.0 V)	Up
High Impedance	No Scan

The input voltage level must be held for a minimum of two clock cycles to insure the desired up or down count. At reset, the latch is taken to the scan-up state.

BCD UP/DOWN COUNTER – The BCD Up/Down Counter counts in the range from 00 through 99 and supplies BCD information to the channel-display multiplexing circuitry and the channel ROM. The counter scans the channels at a rate of either one every 30, 8, or 1 clock cycle (2, 7.5, or 60 channels per second for a 60 Hz signal at AC, pin 14):

1) Invalid channels are scanned at a rate of one per clock cycle (60 channels per second for 60 Hz at AC).
2) Valid channels are scanned at a rate of one per 30 clock cycles (2 channels per second for 60 Hz at AC).
3) If the channel-scan key is depressed (i.e., Ch, pin 16, is taken either low or high) for more than 120 clock cycles, the valid channels are scanned at a rate of one per 8 clock cycles (7.5 channels per second for 60 Hz at AC).

The channel-scan function is shown in the flowchart in Figure 2. A list of the valid channels programmed into the MC6195 is given in Table 1; Table 2 is a list of valid channels programmed into the MC6196.

At reset, the counter is taken to zero. If, during scanning, the On/Off Latch is changed to the OFF state, the counter stops but maintains its present state.

CLOCK – The Clock provides timing for the BCD Up/Down Counter.

PHASE-LOCKED LOOP OPERATION

CHANNEL ROM – The Channel ROM is a 100- by 15-bit channel-conversion ROM, which converts the BCD channel number from the BCD Up/Down Counter into the preset code (for the 12-bit programmable divider) corresponding to the selected valid channel.

12-BIT PROGRAMMABLE DIVIDER – The 12-bit Programmable Divider divides the prescaled local oscillator frequency at f_{in} (pin 20) by the programmed value supplied by the Channel ROM. The output of the divider goes to one in-

FIGURE 1 — FLOWCHART SHOWING THE RELATIONSHIP OF TMO, ONRM, AND THE STATE OF THE ON/OFF LATCH

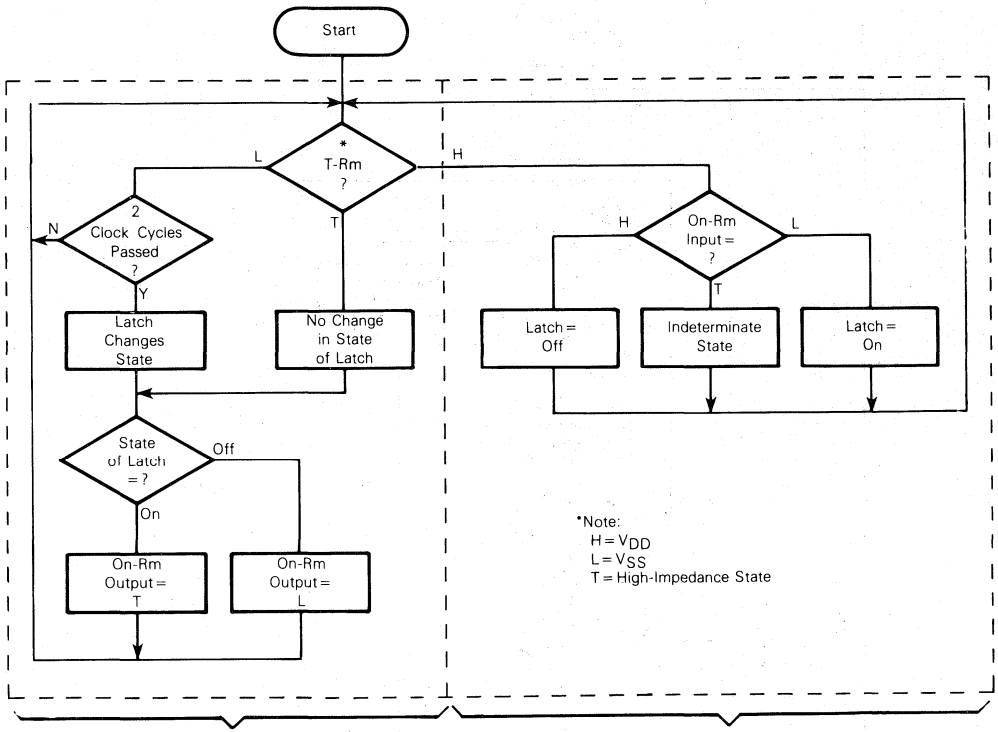


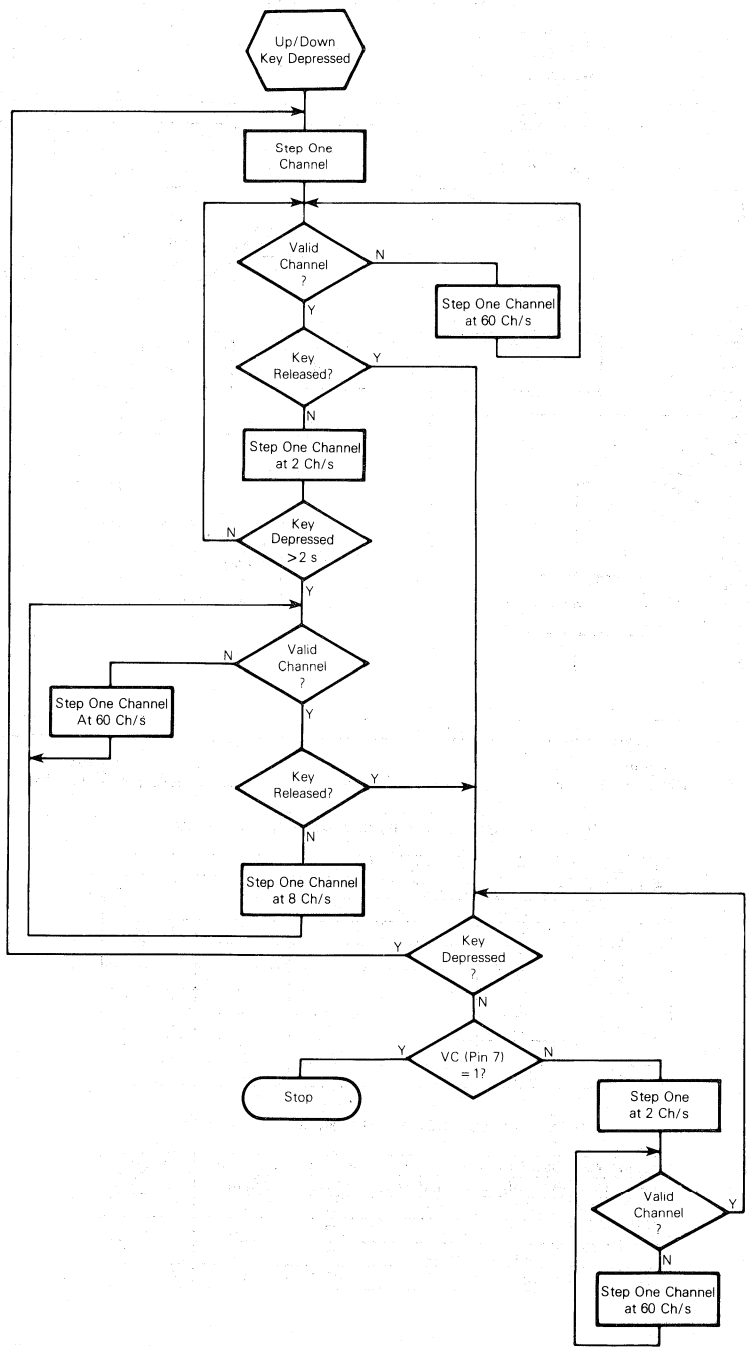
TABLE 1 — FREQUENCY ASSIGNMENTS FOR THE MC6195

Channel Nos.		Osc Freq	Osc Freq	Divide No.	Divide No.	Band	
Start	Stop	Start (MHz)	Delta (MHz)	Start	Delta	VH	VL
00	01	722	6	361	3	1	1
02	04	668	6	334	3	1	1
05	06	690	6	345	3	1	0
07	13	788	6	394	3	1	1
14	22	734	6	367	3	1	1
23	36	830	6	415	3	1	1
37	53	914	6	457	3	0	1
54	59	686	6	343	3	0	1

TABLE 2 — FREQUENCY ASSIGNMENTS FOR THE MC6196

Channel Nos.		Osc. Freq.	Osc. Freq.	Divide No.	Divide No.	Band	
Start	Stop	Start (MHz)	Delta (MHz)	Start	Delta	VL	VH
02	04	101	6	101	6	1	0
05	06	123	6	123	6	1	0
07	13	221	6	221	6	0	1
14	83	517	6	517	6	0	0

FIGURE 2 — OPERATION OF THE CHANNEL-SCAN CIRCUITRY FOR AC (PIN 14) = 60 Hz



put of the Phase Detector, to be compared to the reference frequency.

REFERENCE OSCILLATOR – The Reference Oscillator circuit consists of an inverter and resistor internal to the device, and requires an external crystal. For critical applications, capacitors from Osc_{in} and Osc_{out} to ground can provide the crystal with the optimum capacitive load.

Depending upon the mask option chosen, either a 4 MHz or a 3.57954 MHz reference crystal may be used.

12-BIT PROGRAMMABLE REFERENCE DIVIDER – The 12-Bit Programmable Reference Divider divides the Reference Oscillator frequency by a number that has been programmed at the mask level. The output of the Reference Divider goes to one input of the Phase Detector, to act as the reference frequency.

PHASE DETECTOR – The Phase Detector compares the signal from the 12-bit Programmable Divider to the signal from the 12-Bit Programmable Reference Divider and gives an output that is the phase difference between the two signals. The output of the Phase Detector goes to the AFT Switch.

AFT SWITCH OPERATION

The AFT Switch is controlled by the AFT input pin (pin 6).

When AFT is open-circuit, the device is in the AFT mode. In this mode, PD (pin 5) becomes the output of the Phase Detector and supplies the tuning voltage to the external linear amplifier. Thus, the internal phase-locked loop circuitry forces the change to the desired channel. Then, when video coincidence is detected at the VC input (pin 7), receiver lock is indicated, and receiver control is switched to the external receiver AFT circuits.

In a typical application, the receiver AFT circuit is built into the system with a nominal reference voltage of 1.3 volts. The dynamic range should be ±1.0 volt from this nominal value with a positive voltage (referenced to 1.3 volts) for positive frequency error and a negative voltage for negative frequency error.

The external AFT circuit retains control until loss of video coincidence occurs or a channel change is begun. In the AFT mode, the phase-locked loop regains control by an internal pull-down circuit. Proper operation of this pull-down circuit requires the VC input to be current-limited to 200 μA.

When the AFT input pin is taken to V_{SS}, the device is in the non-AFT mode, and PD (pin 5) is switched to a high-impedance state.

DISPLAY SECTION

ZERO CROSSING DETECTOR – The Zero Crossing Detector is a hysteresis gate with a threshold voltage of about 1 volt, and is used to multiplex the display LEDs.

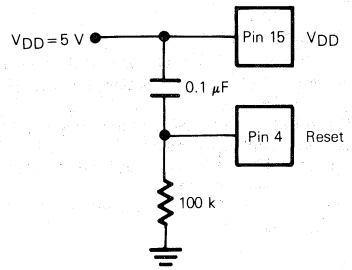
DISPLAY MULTIPLEXER – The Display Multiplexer provides the BCD data to the A, B, C, and D output pins. When AC (pin 14) is high (V_{DD}), the data outputs display the most significant digit of the channel number. When AC is low (V_{SS}), the data outputs display the least significant digit. The display is blanked when the On/Off Latch is in the OFF state.

The Display Multiplexer has a sinking capability of 1.6 mA at 0.4 volts, and can interface with TTL and LSTTL logic.

START-UP AND POWER-ON RESET

When power is applied to the chip, reset is generated (See Figure 3). The BCD Up/Down Counter is reset and begins the channel-scan operation, stopping at the lowest valid channel. The display is blanked. When the input at T-Rm (pin 17) takes the On/Off Latch to either the ON state or the remote-control state, the display is activated and the lowest valid channel number is displayed.

FIGURE 3 – POWER-ON RESET EXTERNAL CIRCUIT



TEST MODE

If SS (pin 19) is forced high during the channel-scan operation, Test Mode is started.

PIN DESCRIPTIONS

V_{SS} (PIN 1)

V_{SS} is the negative power supply pin, usually ground.

Osc_{out} (PIN 2)

Osc_{out} is the output of the oscillator circuit.

Osc_{in} (PIN 3)

Osc_{in} is the input of the oscillator circuit.

Reset (PIN 4)

Reset is the input for power-on reset. It is normally tied to V_{DD} through a 0.1 μf capacitor. (See Figure 3).

PD (PIN 5)

PD is the output of the phase detector.

AFT (PIN 6)

AFT is the AFT control input pin, which is either left open-circuited or tied to ground.

VC (PIN 7)

This is the video coincidence input from the linear amplifier. A high logic level (V_{DD}) supplied to this pin indicates receiver lock.

VL (PIN 8)

VL is the VHF low-band output. It is an open-drain N-channel that can act only as a current sink. This output is accessed by the channel ROM and is normally used for band switching.

VH (PIN 9)

VH is the VHF high-band output. It is an open-drain N-channel that can act only as a current sink. This output is accessed by the channel ROM and is normally used for band switching.

A, B, C, D (PINS 13, 12, 11, 10)

These inputs normally are multiplexed BCD data outputs for channel display. They may, however, be used as inputs for presetting channel values.

The AC and Reset inputs are used to strobe in the preset channel data in the following manner:

1) The logical AND of $\overline{AC}$ and Reset enables the preset of the MSD of the channel number.

2) The logical AND of AC and Reset enables the preset of the LSD of the channel number.

AC (PIN 14)

AC is the ac voltage input, which provides the internal system clock for the multiplexed data output pins and the channel scanning operation.

An internal clamp limits the voltage swing at this input to a value between −0.60 and 5 volts. If the input goes below ground, an internal diode clamps to, typically, −0.6 volts. A normal input to this pin is a 12 VRMS (17 V p-p sine wave), current limited with a series resistor to 200 μA. For the internal clamps to work properly, the input level must be current limited.

V_{DD} (PIN 15)

V_{DD} is the positive power supply pin, typically +5 volts.

Ch (PIN 16)

Ch is the three-state input pin that determines the direction of channel scan (scan up or scan down).

T-Rm (PIN 17)

Toggle or Remote Input — T-Rm is a three-state input pin that may either toggle the On/Off Latch or permit remote operation (See Figure 1). Normally, the pin is left in the high-impedance state and there is no On/Off operation.

On-Rm (PIN 18)

On-Rm is either the three-state output from the On/Off Latch or the input to the On/Off Latch from the remote-control receiver (See Figure 1).

SS (PIN 19)

SS is an open drain output that goes low during channel scanning. It is also used as an input for the LSI Test Mode.

f_{in} (PIN 20)

f_{in} is the input pin that receives the prescaled local oscillator frequency. Internal circuitry provides dc bias to the f_{in} input so that the prescaled local oscillator frequency can be ac coupled. If this input is to be dc coupled, standard TTL input voltages are required for logic levels.

APPLICATIONS

A system constructed with the MC6195 PLL frequency synthesizer chip, a CATV up converter, and a minimum number of external components, is shown in Figure 4; a system using the MC6196 PLL, a linear control chip, and external components is shown in Figure 5.

MC2801 LINEAR CONTROL CHIP — This linear control chip integrates all the control circuits and regulators required in the system on a single chip.

The filter amplifier provides active filtering in the PLL network. The output of this amplifier, PD, drives the tuner varicap diodes. The non-inverting input of this amplifier, "NI", is internally biased with the AFT reference voltage (1.3 volts) to simplify the external circuitry. This bias voltage, however, can be externally changed with a single resistor, if required.

A high-voltage regulator provides up to 34 volts for the filter amplifier.

The coincidence output "CO", will go high when the video sync/signal (in video input, "VI") and the fly back pulse (in fly back input, "FI") are synchronized. "CO" detects channel lock.

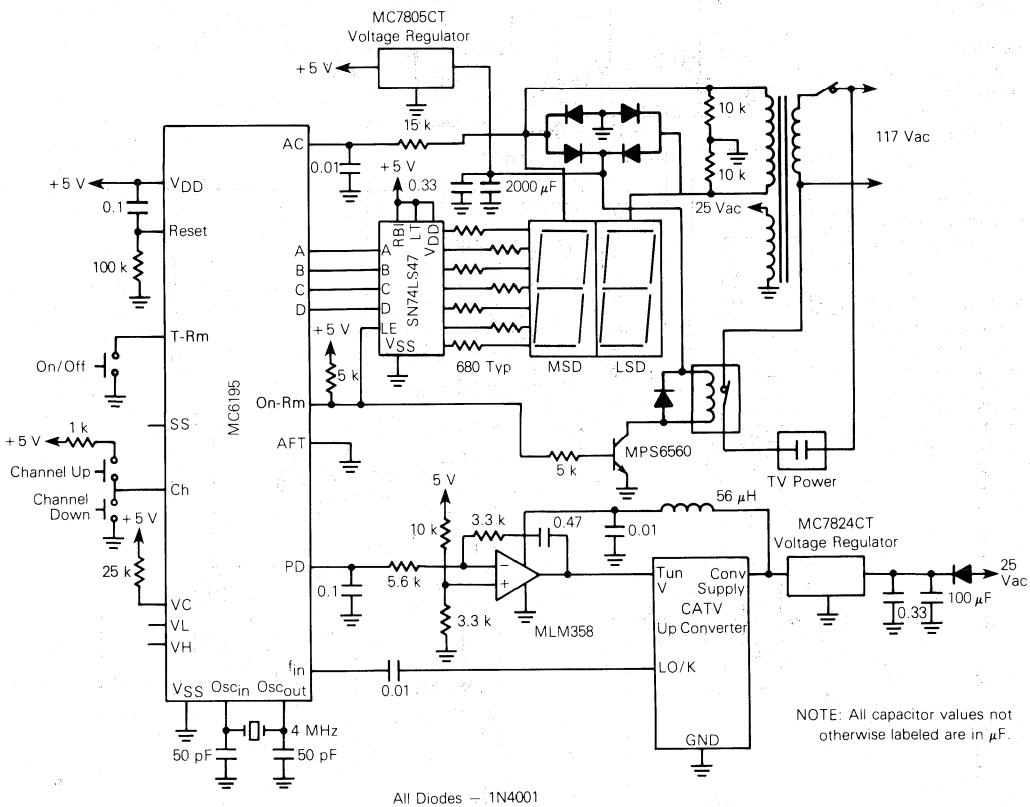
The band-switch circuit decodes band-select information and provides constant-current output to an external transistor for band-switching operation. The decoding format is shown below:

VH Input	VL Input	Selected Band
0	0	UHF Band
1	0	VHF High Band
0	1	VHF Low Band

The low-voltage regulator section provides a regulated 5 volts to the MC6196 and the other circuits, with current limiting capability. The output current rating is determined by the external series pass transistor.

MC12071 PRESCALER — The ECL prescaler may be used to count down the local oscillator frequency by 256 for UHF and VHF, to supply an incoming frequency of less than 4.1 MHz to the PLL programmable divider.

FIGURE 4 – CATV TUNING SYSTEM BLOCK DIAGRAM



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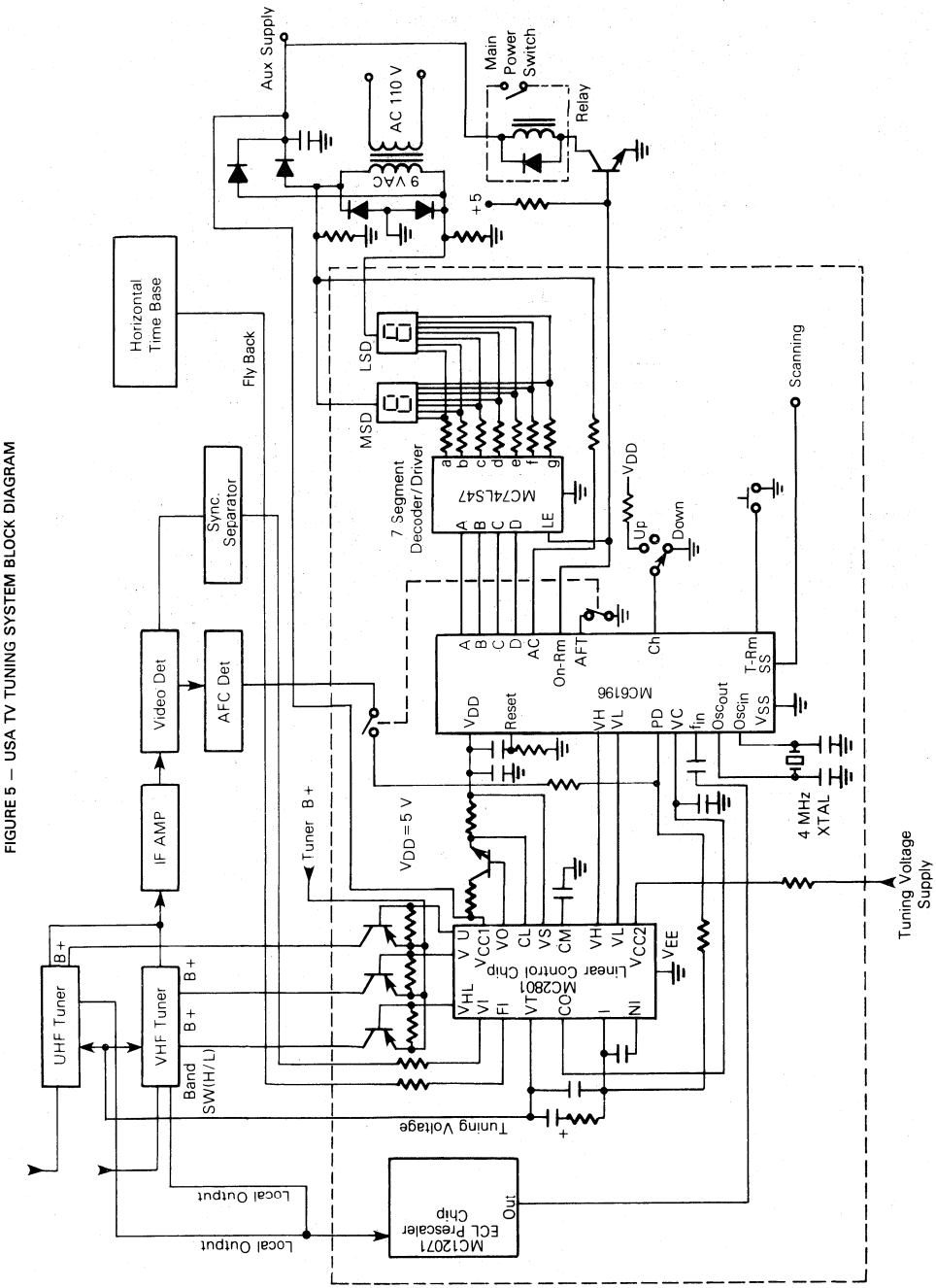


FIGURE 5 — USA TV TUNING SYSTEM BLOCK DIAGRAM

MOTOROLA

MC14046B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

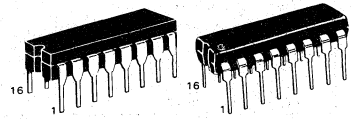
PHASE LOCKED LOOP

PHASE LOCKED LOOP

The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90^o phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, $PC2_{out}$ and LD, and maintains a 0^o phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- VCO Frequency = 1.4 MHz Typical @ V_{DD} = 10 V
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ V_{DD} = 10 V
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 V
- Low Dynamic Power Dissipation — 70 μW Typical @ f_0 = 10 kHz, V_{DD} = 5.0 V, R1 = 1.0 MΩ, R2 = ∞, R_{SF} = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited



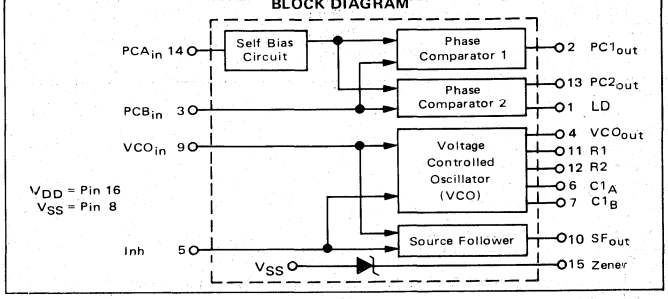
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

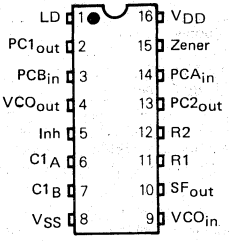
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



PIN ASSIGNMENT



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MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Input Current, per Pin	I_{in}	±10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 V)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 V)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 V)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 V)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 V)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 V)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µA
(Per Package) Inh = PCA_{in} = V_{DD},		10	–	10	–	0.010	10	–	300	
Zener = VCO_{in} = 0 V, PCB_{in} = V_{DD}		15	–	20	–	0.015	20	–	600	
or 0 V, I_{out} = 0 µA										
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.010	20	–	150	µA
(Per Package) Inh = PCA_{in} = V_{DD},		10	–	40	–	0.020	40	–	300	
Zener = VCO_{in} = 0 V, PCB_{in} = V_{DD}		15	–	80	–	0.040	80	–	600	
or 0 V, I_{out} = 0 µA										
Total Supply Current †	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µA
(Inh = "0", f_o = 10 kHz, C_L = 50 pF,		10	I_T = (2.91 µA/kHz) f + I_{DD}							
R1 = 1 MΩ, R2 = ∞, R_{SF} = ∞, and		15	I_T = (4.37 µA/kHz) f + I_{DD}							
50% Duty Cycle)										

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD}\left(\frac{VCO_{in}-1.65}{R1}+\frac{V_{DD}-1.35}{R2}\right)^{3/4} + 1.6\times\left(\frac{VCO_{in}-1.65}{R_{SF}}\right)^{3/4} + 1\times10^{-3}(C_L+9)V_{DD}\,f + 1\times10^{-1}V_{DD}^2\left(\frac{100\text{ -\% Duty Cycle of }PCA_{in}}{100}\right)+I_Q$$

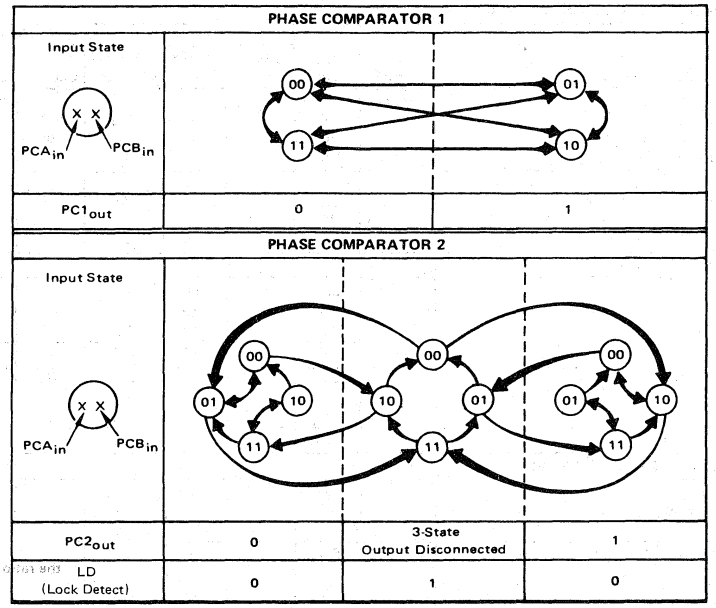
where: I_T in µA, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in KHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Units
Output Rise Time	t_{TLH}							ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_{THL}							ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
PHASE COMPARATORS 1 and 2								
Input Resistance – PCA_{in}	R_{in}	5.0	1.0	1.0	2.0	–	–	MΩ
		10	0.2	0.2	0.4	–	–	
		15	0.1	0.1	0.2	–	–	
– PCB_{in}	R_{in}	15	150	15	1500	–	–	MΩ
Minimum Input Sensitivity	V_{in}	5.0	–	–	200	300	400	mV p-p
AC Coupled – PCA_{in}		10	–	–	400	600	800	
C series = 1000 pF, f = 50 kHz		15	–	–	700	1050	1400	
DC Coupled – PCA_{in}, PCB_{in}	–	5 to 15	See Noise Immunity					
VOLTAGE CONTROLLED OSCILLATOR (VCO)								
Maximum Frequency	f_{max}	5.0	0.50	0.35	0.70	–	–	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF,		10	1.0	0.7	1.4	–	–	
R1 = 5 kΩ, and R2 = ∞)		15	1.4	1.0	1.9	–	–	
Temperature – Frequency Stability	–	5.0	–	–	0.12	–	–	%/°C
(R2 = ∞)		10	–	–	0.04	–	–	
		15	–	0	0.015	–	10	
Linearity (R2 = ∞)	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R1 ≥ 10 kΩ)		5.0	–	–	1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R1 ≥ 400 kΩ)		10	–	–	1	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R1 ≥ 1000 kΩ)		15	–	–	1	–	–	
Output Duty Cycle	–	5 to 15	–	–	50	–	–	%
Input Resistance – VCO_{in}	R_{in}	15	150	50	1500	–	–	MΩ
SOURCE-FOLLOWER								
Offset Voltage	–	5.0	–	–	1.65	2.2	2.5	V
(VCO_{in} minus SF_{out}, R_{SF} > 500 kΩ)		10	–	–	1.65	2.2	2.5	
		15	–	–	1.65	2.2	2.5	
Linearity	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R_{SF} > 50 kΩ)		5.0	–	–	0.1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R_{SF} > 50 kΩ)		10	–	–	0.6	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R_{SF} > 50 kΩ)		15	–	–	0.8	–	–	
ZENER DIODE								
Zener Voltage (I_Z = 50 μA)	V_Z	–	6.7	6.3	7.0	7.3	7.7	V
Dynamic Resistance (I_Z = 1 mA)	R_Z	–	–	–	100	–	–	Ω

*The formula given is for the typical characteristics only.

FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS



Refer to Waveforms in Figure 3.

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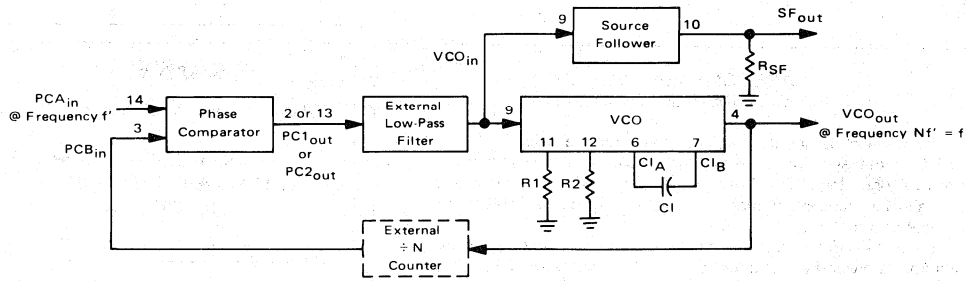
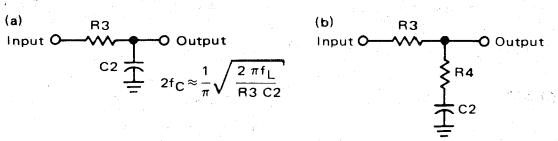
FIGURE 2 – DESIGN INFORMATION

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). $f_C < f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is less than ±20%.	$f_{min} = \frac{1}{R_2(C_1 + 32\ pF)}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32\ pF)} + f_{min}$ (V_{CO} input = V_{DD}) Where: $10K < R_1 < 1M$ $10K < R_2 < 1M$ $100pF < C_1 < .01\ \mu F$	

FIGURE 3 – GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi\Delta f}$$

$$(R_3 + 3{,}000\Omega)\ C_2 = \frac{100N\Delta f}{f_{max}^2} - R_4 C_2$$

$$\Delta f = f_{max} - f_{min}$$

Note: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor C_C is then placed from the midpoint to ground. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_n. In Figure B, the ratio of R3 to R4 sets the damping, R4 ≅ (0.1)(R3) for optimum results.

Definitions: N = Total division ratio in feedback loop

$K\phi = V_{DD}/\pi$ for Phase Comparator 1

$K\phi = V_{DD}/4\pi$ for Phase Comparator 2

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{V_{DD} - 2\ V}$$

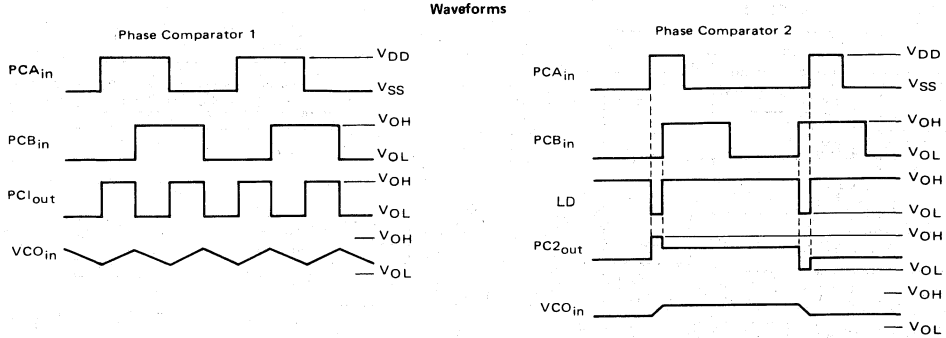
for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input)

$\zeta \cong 0.707$

LOW-PASS FILTER

Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{NR_3C_2}}$	$\omega_n = \sqrt{\frac{K\phi K_{VCO}}{NC_2(R_3+R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi K_{VCO}}$	$\zeta = 0.5\ \omega_n(R_3C_2 + \frac{N}{K\phi K_{VCO}})$
$F(s) = \frac{1}{R_3C_2S+1}$	$F(s) = \frac{R_3C_2S+1}{S(R_3C_2+R_4C_2)+1}$

Waveforms



Note: for further information, see:

(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.

(2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

(3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.

6

MOTOROLA

MC14568B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

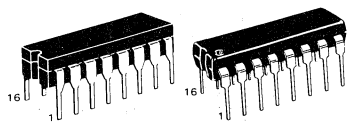
PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/or high noise immunity.

This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used independently of the programmable divide-by-N counter, for example cascaded with a MC14569B, MC14522B or MC14526B (CTL low).

- Quiescent Current = 5.0 nA typ/pkg @ 5 V
- Supply Voltage Range = 3.0 to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Chip Complexity: 549 FETs or 137 Equivalent Gates



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

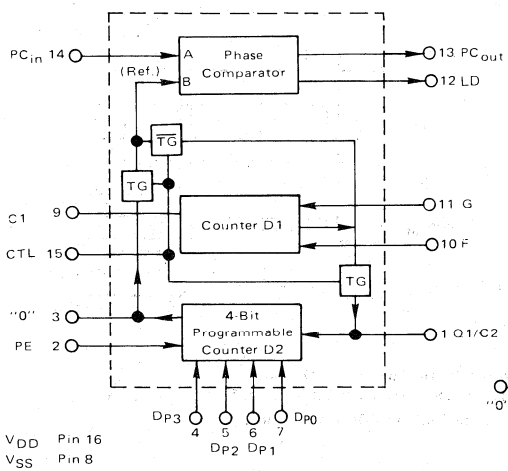
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

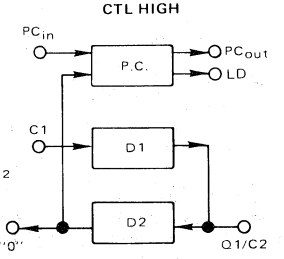
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.

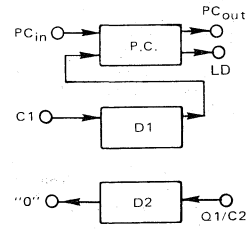
BLOCK DIAGRAM



CTL HIGH



CTL LOW



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

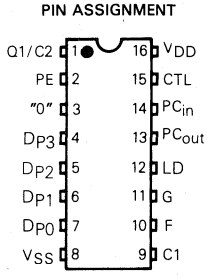
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage#† "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package) V_{in}=0 or V_{DD},		10	–	10	–	0.010	10	–	300	
I_{out}=0 µA		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package) V_{in}=0 or V_{DD},		10	–	40	–	0.010	40	–	300	
I_{out}=0 µA		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.4 µA/kHz) f + I_{DD}							
		15	I_T = (0.9 µA/kHz) f + I_{DD}							
Three-State Leakage Current, Pins 1, 13 (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current, Pins 1, 13 (CL/CP Devices)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

†Pin 15 is connected to V_{SS} or V_{DD} for input voltage test.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	180	360	ns
		10	–	90	180	
		15	–	65	130	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Pulse Width, C1, Q1/C2, or PC_{in} Input	t_{WH}	5.0	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
Maximum Clock Rise and Fall Time, C1, Q1/C2, or PC_{in} Input	t_{TLH}, t_{THL}	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
PHASE COMPARATOR						
Input Resistance	R_{in}	5.0 to 15	–	10^6	–	MΩ
Input Sensitivity, dc Coupled	–	5.0 to 15	See Input Voltage			
Turn-Off Delay Time, PC_{out} and LD Outputs	t_{PHL}	5.0	–	550	1100	ns
		10	–	195	390	
		15	–	120	240	
Turn-On Delay Time, PC_{out} and LD Outputs	t_{PHL}	5.0	–	675	1350	ns
		10	–	300	600	
		15	–	190	380	
DIVIDE-BY-4, 16, 64 OR 100 COUNTER (D1)						
Maximum Clock Pulse Frequency	f_{cl}					MHz
Division Ratio = 4, 64 or 100		5.0	3.0	6.0	–	
		10	8.0	16	–	
		15	10	22	–	
Division Ratio = 16		5.0	1.0	2.5	–	
		10	3.0	6.3	–	
		15	5.0	9.7	–	
Propagation Delay Time, Q1/C2 Output	t_{PLH}, t_{PHL}					ns
Division Ratio = 4, 64 or 100		5.0	–	450	900	
		10	–	190	380	
		15	–	130	260	
Division Ratio = 16		5.0	–	720	1440	
		10	–	300	600	
		15	–	200	400	
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)						
Maximum Clock Pulse Frequency (Figure 3a)	f_{cl}	5.0	1.2	1.8	–	MHz
		10	3.0	8.5	–	
		15	4.0	12	–	
Turn-On Delay Time, "0" Output (Figure 3a)	t_{PLH}	5.0	–	450	900	ns
		10	–	190	380	
		15	–	130	260	
Turn-Off Delay Time, "0" Output (Figure 3a)	t_{PHL}	5.0	–	225	450	ns
		10	–	85	170	
		15	–	60	150	
Minimum Preset Enable Pulse Width	$t_{WH(PE)}$	5.0	–	75	250	ns
		10	–	40	100	
		15	–	30	75	

6

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – PHASE COMPARATOR

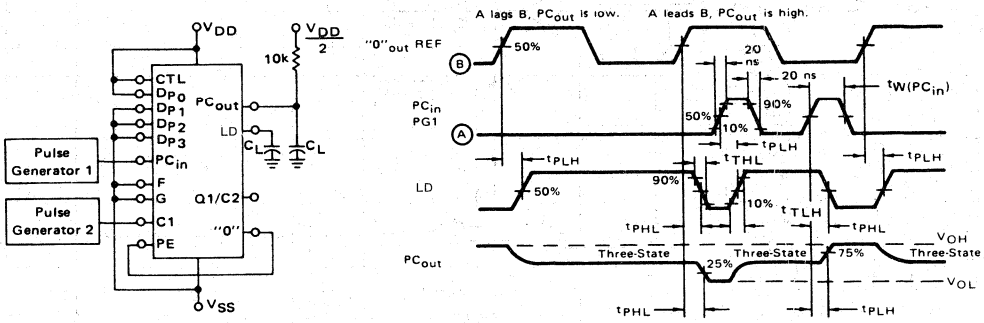


FIGURE 2 – COUNTER D1

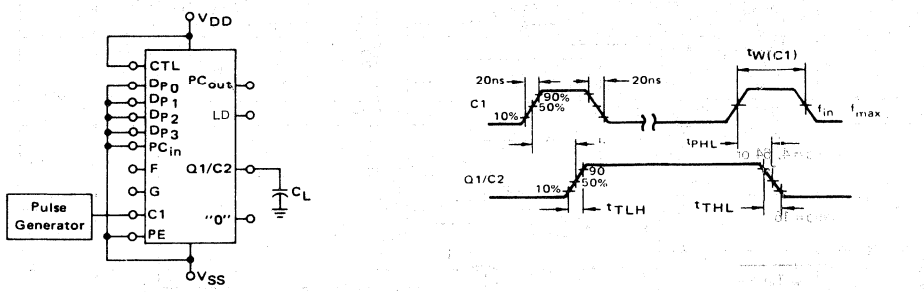
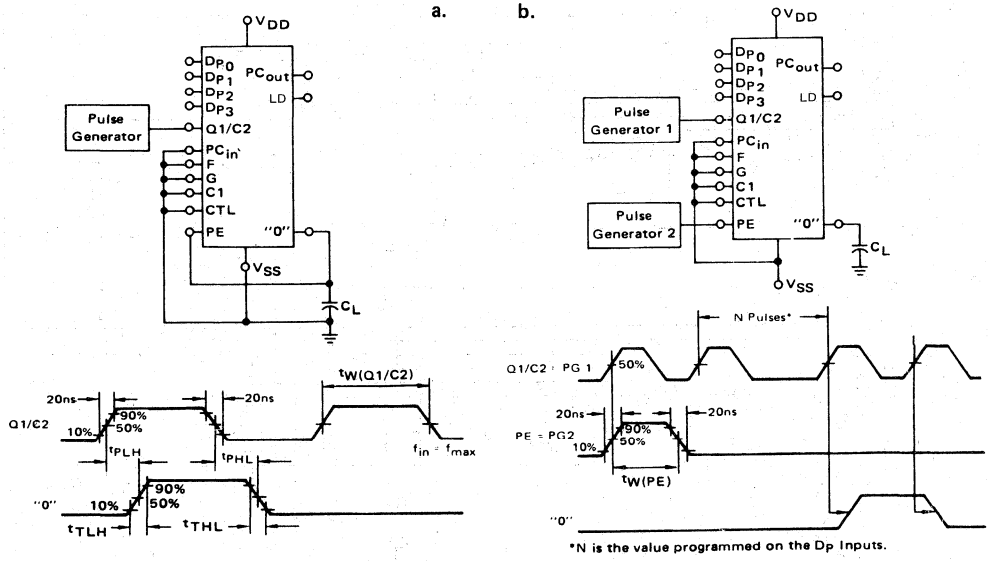
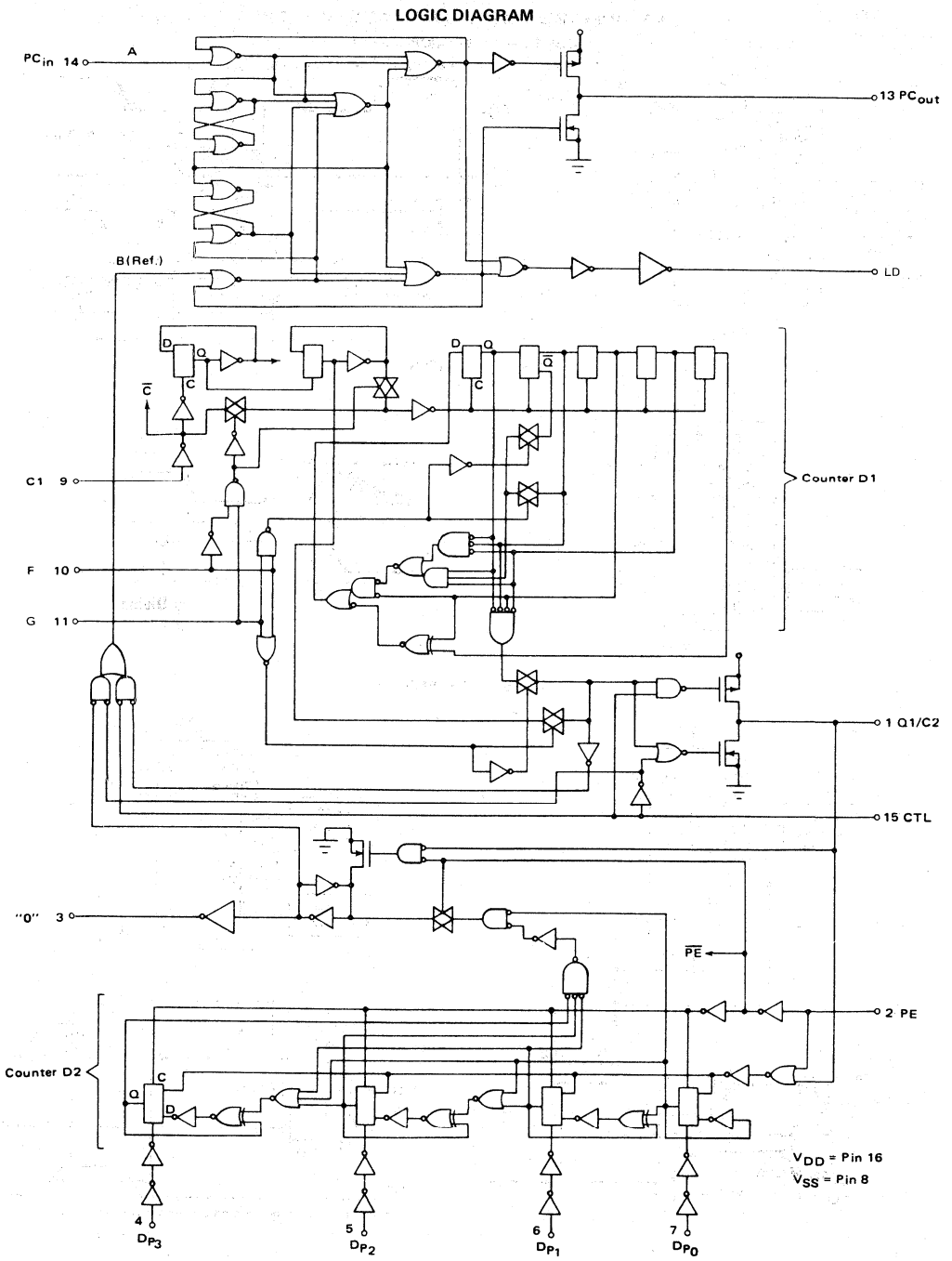


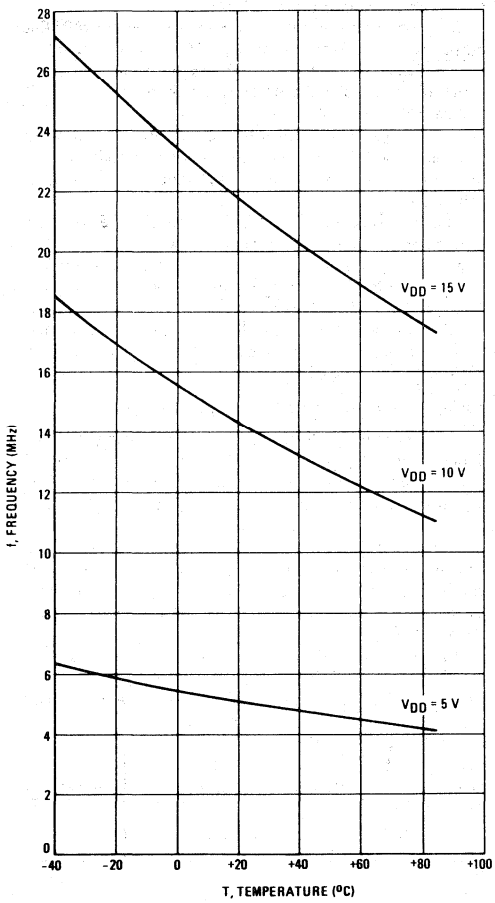
FIGURE 3 – COUNTER D2



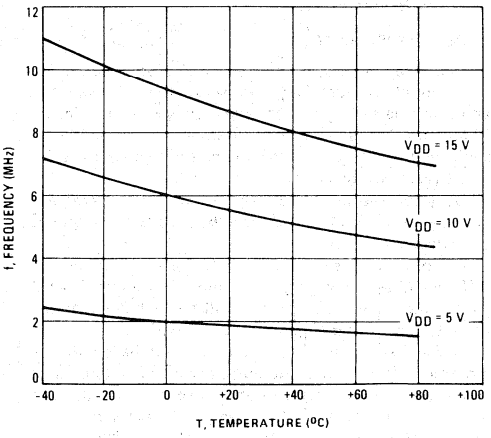
LOGIC DIAGRAM



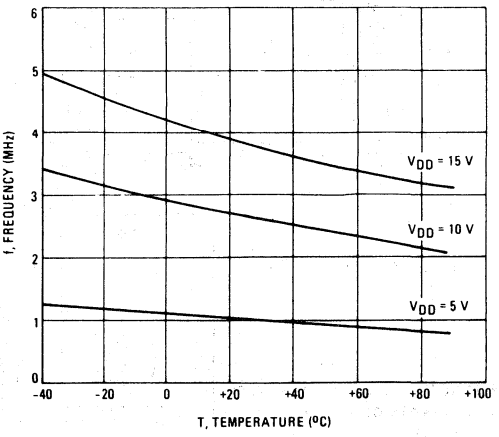
Typical Maximum Frequency Divider D1
Division ratios: 4, 64 or 100 (CL = 50 pF)



Typical Maximum Frequency Divider D1
Division ratio: 16 (CL = 50 pF)



Typical Maximum Frequency Divider D2
Division ratio: 2 (CL = 50 pF)



6

OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider (÷ 4, ÷ 16, ÷ 64, ÷ 100) and a programmable divide-by-N 4-bit counter.

PHASE COMPARATOR

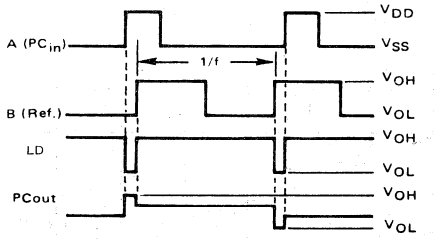
The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

FIGURE 4 – PHASE COMPARATOR WAVEFORMS



If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A, and low otherwise.

Under the same conditions of frequency difference, the output will vary between V_{OH} (or V_{OL}) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

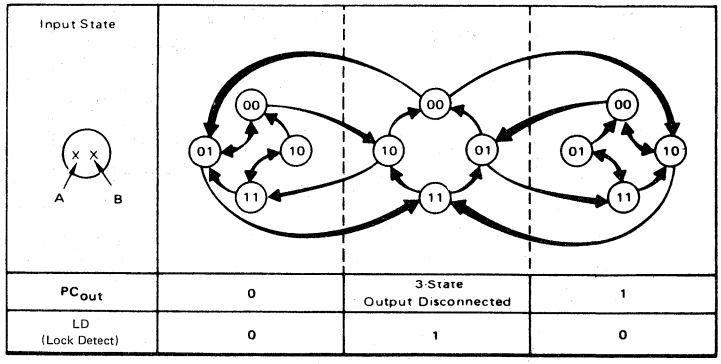
The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies.

DIVIDE BY 4, 16, 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to V_{DD} allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS}.

The different division ratios have been chosen to generate the reference frequences corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.

FIGURE 5 – PHASE COMPARATOR STATE DIAGRAM



PC_{out}	0	3-State Output Disconnected	1
LD (Lock Detect)	0	1	0

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs D_{P0} . . . D_{P3} (pins 7 . . . 4). The Preset Enable input enables the parallel preset inputs D_{P0} . . . D_{P3}. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

TYPICAL APPLICATIONS

FIGURE 6 – CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

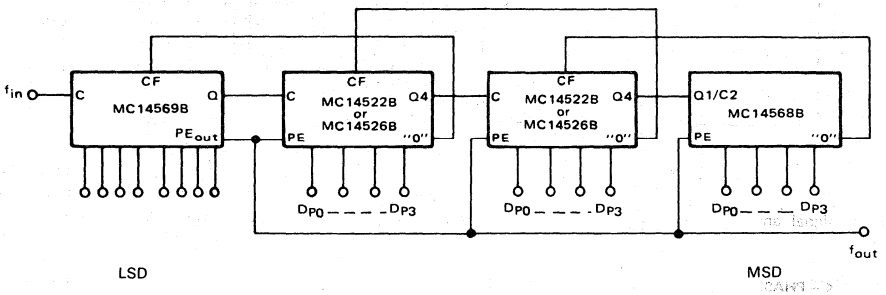
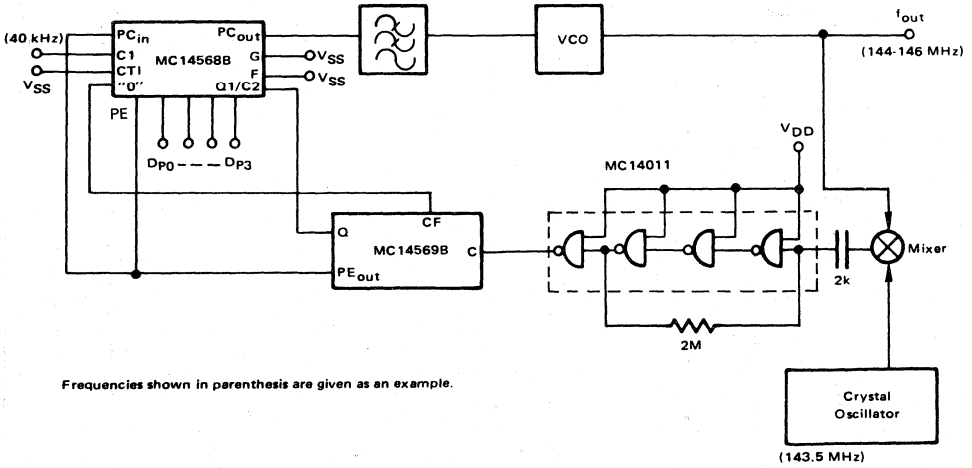
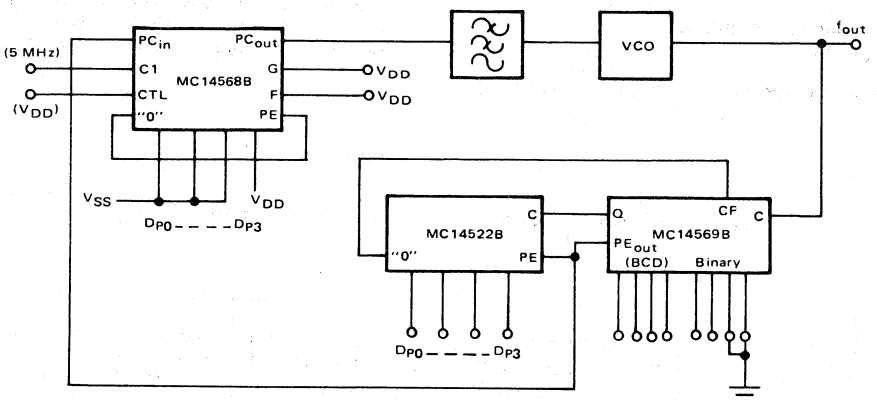


FIGURE 7 – FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example.

FIGURE 8 – FREQUENCY SYNTHESIZER USING MC14568B, MC14569B AND MC14522B
(Without Mixer)



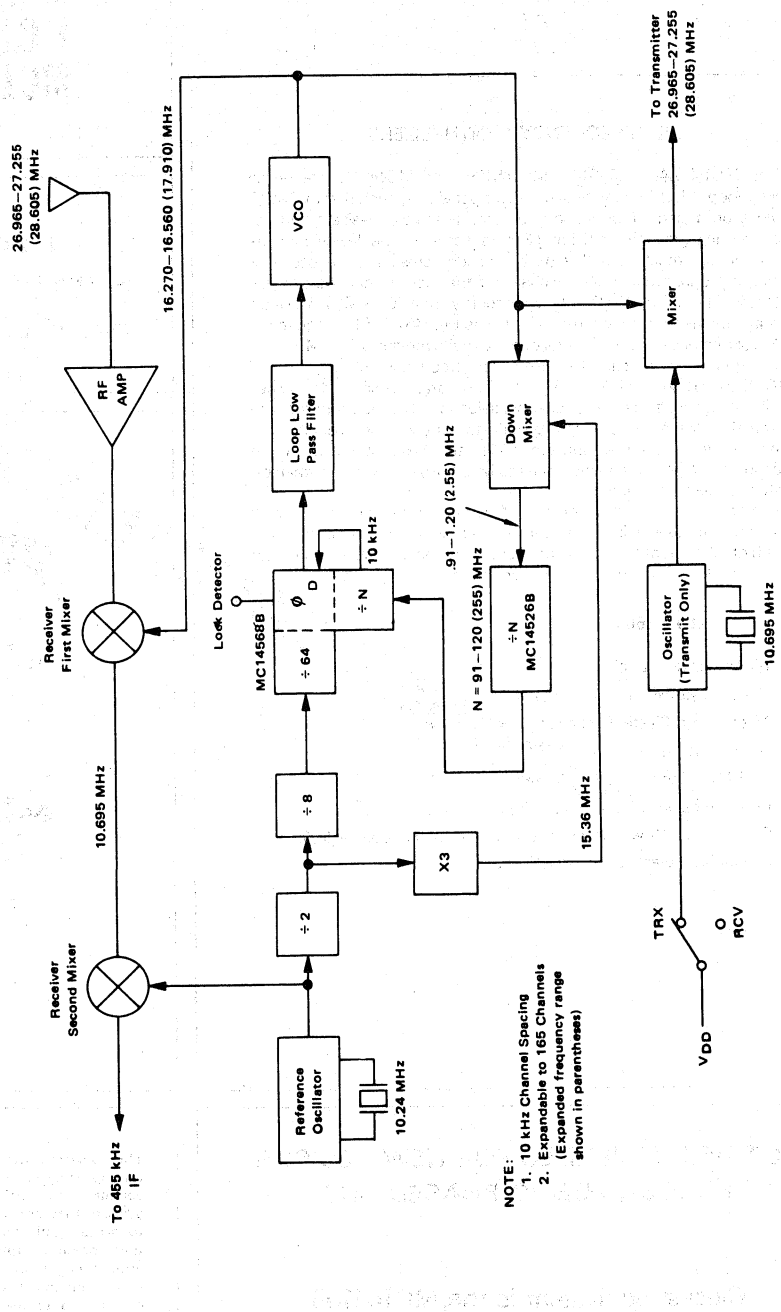
N_1	N_2	N_3
(0–5)	(0–9)	(0, 4, 8, 12)
(625 kHz steps)	(62.5 kHz steps)	(6.25 kHz steps)

Divide ratio = $160N_1 + 16N_2 + N_3$

Example:
$f_{out} = N_1$ (MHz) + N_2 (x100 kHz) + N_3 (x25 kHz)
Frequency range = 5 MHz
Channel spacing = 25 kHz
Reference frequency = 6.25 kHz

Figures shown in parenthesis refer to example.

FIGURE 9 – TYPICAL 23-CHANNEL CB FREQUENCY SYNTHESIZER FOR DOUBLE CONVERSION TRANSCEIVERS



6

MOTOROLA

MC145104
MC145107
MC145109
MC145112

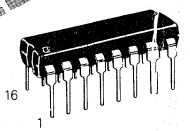
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)
PLL
FREQUENCY SYNTHESIZERS

PLL FREQUENCY SYNTHESIZERS

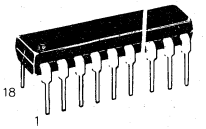
The MC145104, MC145107, MC145109, and MC145112 are phase locked loop (PLL) frequency synthesizer parts constructed with CMOS devices on a single monolithic structure. These synthesizers find applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145104/5112 have circuitry for a 10.24 MHz oscillator or may operate with an external signal. The MC145107/5109 require the external reference signal. Several of the circuits provide a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 (MC145109/5112) or 2^8 (MC145104/5107) programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal provided from the on-chip lock detector with a "0" level for the out of lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- 16 or 18 Pin Plastic Packages
- 10.24 MHz Oscillator on Chip
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11}



P SUFFIX
PLASTIC PACKAGE
CASE 648



P SUFFIX
PLASTIC PACKAGE
CASE 707

NOT RECOMMENDED FOR NEW DESIGNS
PRODUCT BEING PHASED OUT

Closest equivalent is the MC145106

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out} \leq V_{DD}$.

MOTOROLA

MC145106

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

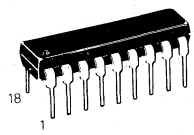
PLL
FREQUENCY SYNTHESIZER

PLL FREQUENCY SYNTHESIZER

The MC145106 is a phase locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

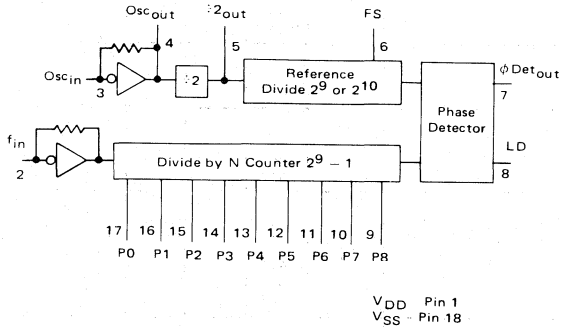
The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (including ÷ 2)
- Three-State Phase Detector
- Pin-for-Pin Replacement for MM55106, MM55116
- Chip Complexity: 880 FETs or 220 Equivalent Gates

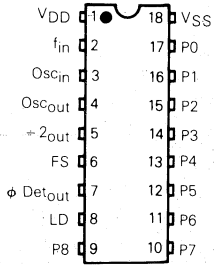


P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM



PIN ASSIGNMENT



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MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +12	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Power Supply Voltage Range		V_{DD}	–	4.5	–	12	V
Supply Current		I_{DD}	5.0	–	6	10	mA
			10	–	20	35	
			12	–	28	50	
Input Voltage	"0" Level	V_{IL}	5.0	–	–	1.5	V
			10	–	–	3.0	
			12	–	–	3.6	
	"1" Level	V_{IH}	5.0	3.5	–	–	
			10	7.0	–	–	
			12	8.4	–	–	
Input Current	"0" Level	I_{in}	5.0	−5.0	−20	−50	μA
(FS, Pull-up Resistor Source Current)			10	−15	−60	−150	
			12	−20	−80	−200	
(P0 to P8)			5.0	–	–	−0.3	
			10	–	–	−0.3	
			12	–	–	−0.3	
(FS)	"1" Level		5.0	–	–	0.3	
			10	–	–	0.3	
			12	–	–	0.3	
(P0 to P8, Pull-down Resistor Sink Current)			5.0	7.5	30	75	
			10	22.5	90	225	
			12	30	120	300	
(Osc_{in}, f_{in})	"0" Level		5.0	−2.0	−6.0	−15	
			10	−6.0	−25	−62	
			12	−9.0	−37	−92	
(Osc_{in}, f_{in})	"1" Level		5.0	2.0	6.0	15	
			10	6.0	25	62	
			12	9.0	37	92	
Output Drive Current		I_{OH}					mA
(V_O = 4.5 V)	Source		5.0	−0.7	−1.4	–	
(V_O = 9.5 V)			10	−1.1	−2.2	–	
(V_O = 11.5 V)			12	−1.5	−3.0	–	
(V_O = 0.5 V)	Sink	I_{OL}	5.0	0.9	1.8	–	
(V_O = 0.5 V)			10	1.4	2.8	–	
(V_O = 0.5 V)			12	2.0	4.0	–	
Input Amplitude		–					Vp-p
(f_{in} @ 4.0 MHz)			–	1.0	0.2	–	Sine
(Osc_{in} @10.24 MHz)			–	1.5	0.3		
Input Resistance		R_{in}					MΩ
(Osc_{in}, f_{in})			5.0	–	1.0	–	
			10	–	0.5	–	
			12	–	–	–	
Input Capacitance		C_{in}					pF
(Osc_{in}, f_{in})			–	–	6.0		
Three State Leakage Current		I_{OZ}					μA
(ϕ Det_{out})			5.0	–	–	1.0	
			10	–	–	1.0	
			12	–	–	1.0	
Input Frequency		f_{in}	4.5	0	–	4.0	MHz
(−40°C to +85°C)			12	0	–	4.0	
Oscillator Frequency		Osc_{in}	4.5	0.1	–	10.24	MHz
(−40°C to +85°C)			12	0.1	–	10.24	

TYPICAL CHARACTERISTICS

FIGURE 1 – MAXIMUM DIVIDER INPUT FREQUENCY versus SUPPLY VOLTAGE

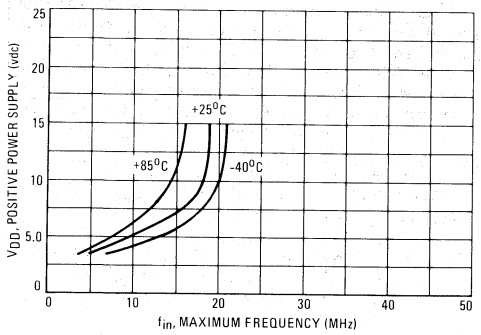
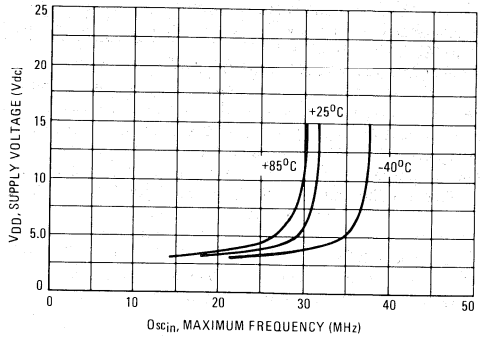


FIGURE 2 – MAXIMUM OSCILLATOR INPUT FREQUENCY versus SUPPLY VOLTAGE



TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide By N
0	0	0	0	0	0	0	0	0	2 (Note 1)
0	0	0	0	0	0	0	0	1	3 (Note 1)
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	1	255
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}
0: Voltage level = 0 or open circuit input

Note 1: The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2^N-1 sequence. When pin is not connected the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8 – Programmable divider inputs (binary)
f_{in} – Frequency input to programmable divider (derived from VCO)
Osc_{in} – Oscillator/amplifier input terminal
Osc_{out} – Oscillator/amplifier output terminal
LD – Lock detector, high when loop is locked, pulses low when out of lock.
ϕ Det_{out} – Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator - input frequency typically 5.0 or 10 kHz.
FS – Reference Oscillator Frequency Division Select. When using 10.24 MHz Osc frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.
$\div 2_{out}$ – Reference Osc frequency divided by 2 output; when using 10.24 MHz Osc frequency, this output is 5.12 MHz for frequency tripling applications.
V_{DD} – Positive power supply
V_{SS} – Ground

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PLL SYNTHESIZER APPLICATIONS

The MC145106 is well suited for applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer, using a single crystal reference, is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145106 can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling and loop programming techniques. In general, 300-400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft synthesizer of Figure 5, the VHF loop (top) will provide a 50 kHz, 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal, 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720 channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transeivers. The VCO operates on frequency during transmit and is offset downward during receive. The offset corresponds to the receiver IF (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 − 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

FIGURE 3 — SINGLE CRYSTAL CB SYNTHESIZER FEATURING ON-FREQUENCY VCO DURING TRANSMIT

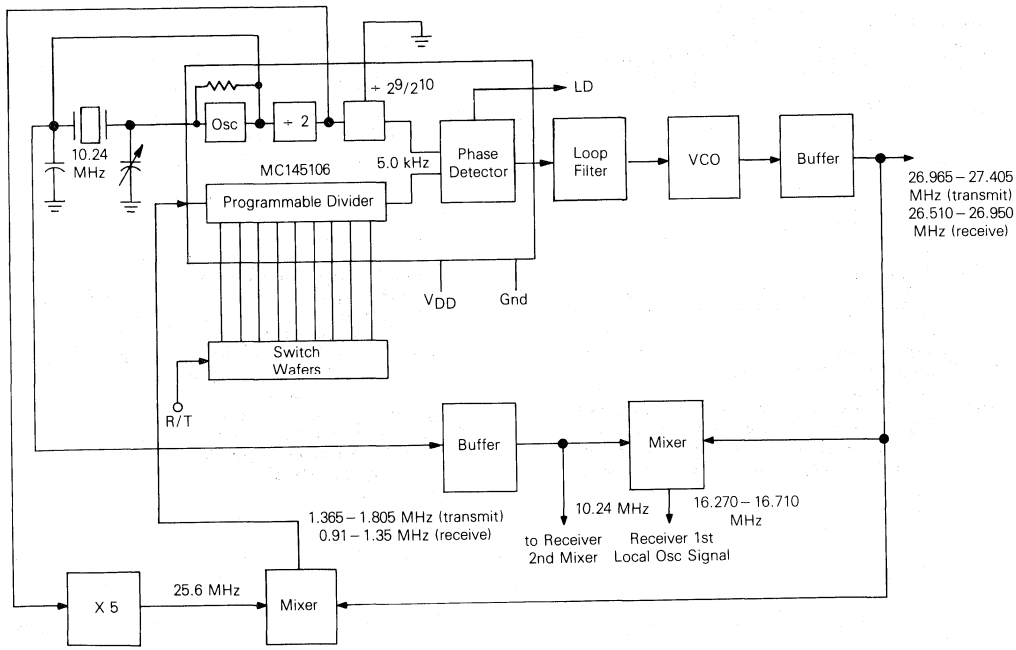
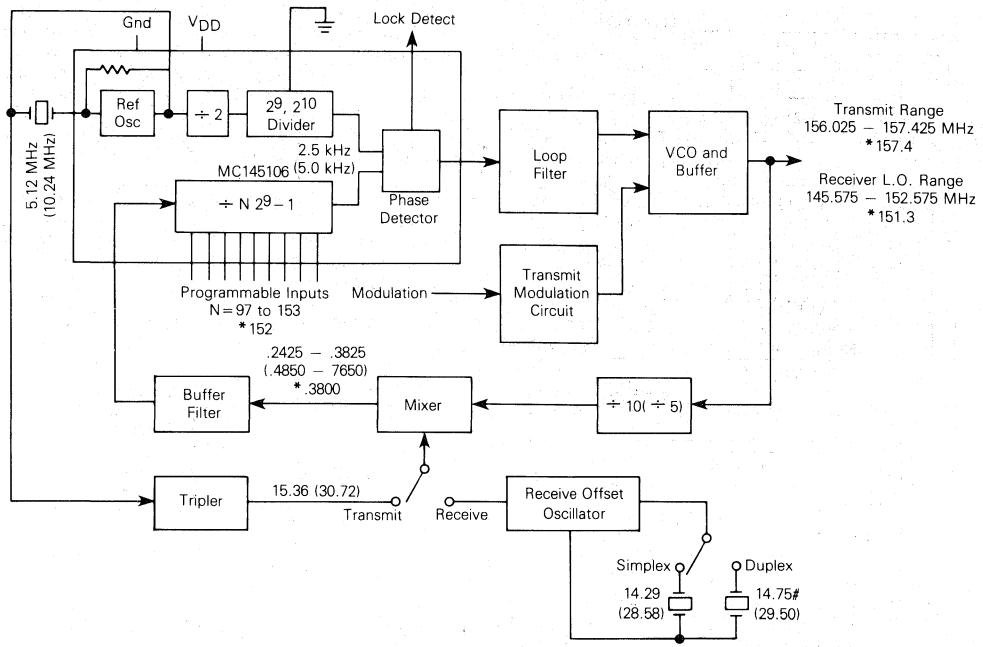


FIGURE 4 — VHF MARINE TRANSCEIVER SYNTHESIZER



NOTES:
- Receiver IF = 10.7 MHz
- Low Side Injection
- Duplex Offset = 4.6 MHz
- Step Size = 25 kHz
- Frequencies in MHz unless noted
- Values in Parentheses are for a 5.0 kHz Reference Frequency
- Example Frequencies for Channel 28 Shown by *

#Can be eliminated by adding 184 to ÷ N for Duplex Channels.

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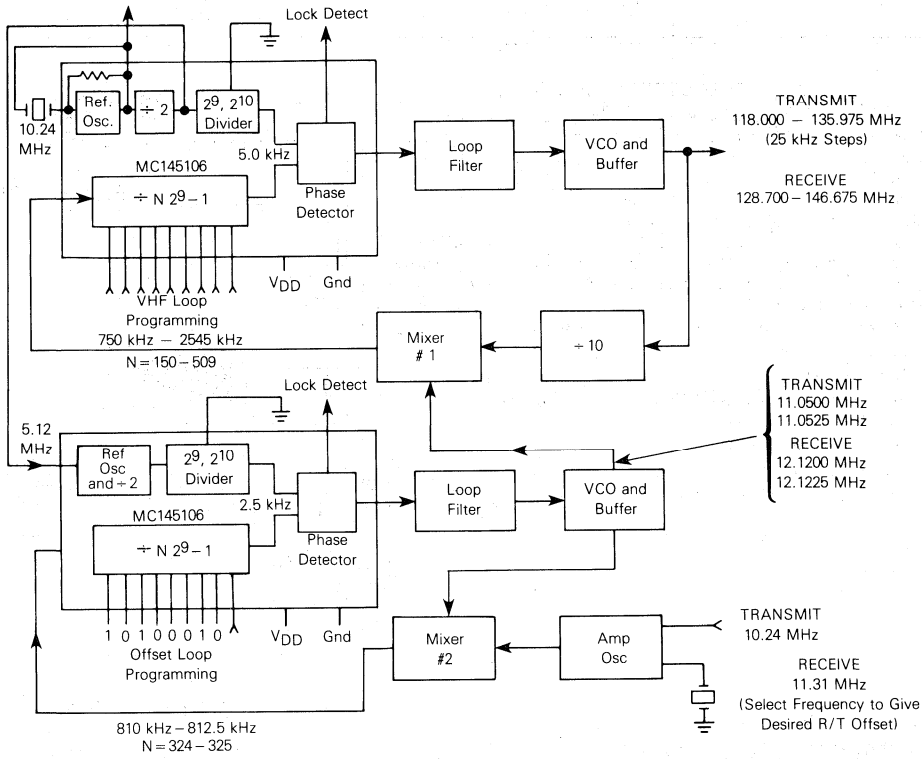
FIGURE 5 — VHF AIRCRAFT 720 CHANNEL TWO CRYSTAL FREQUENCY SYNTHESIZER



MOTOROLA

MC145143

PLL FREQUENCY SYNTHESIZER

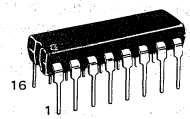
The MC145143 is a phase locked loop building block variation of the MC145106/MC145112 family. The device contains the oscillator circuitry required to operate with fundamental mode crystals to 10.24 MHz. The oscillator circuitry is connected to the phase detector through a divide-by-16 and a 2^9-1 divide-by-N counter. The reference oscillator can be divided in steps of 16 between 32 and 8176 before interfacing with the phase detector. The external input to the phase detector requires a V_{SS} to V_{DD} signal and forces the phase-detector output high if higher in frequency than the output of the divide-by-N counter. An out-of-lock signal is provided from the on-chip lock detector with a "O" level for an out-of-lock condition.

- Operation to 25 MHz
- 4.5 to 12 V Operation
- Programmable Reference Divisions from 32 to 8176 (16×2 to 16×511)
- Three-State Phase Detection
- On-Chip Lock Detection

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PLL
FREQUENCY SYNTHESIZER

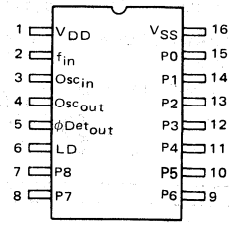


P SUFFIX
PLASTIC PACKAGE
CASE 648

NOT RECOMMENDED FOR NEW DESIGNS
PRODUCT BEING PHASED OUT

Closest equivalent is the MC145106

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

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MOTOROLA

MC145144

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145144 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

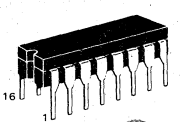
The MC145144 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, programmable reference divider, digital-phase detector, programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145144 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145144.

- Tailored for TV Tuning Applications
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3584 and 3839
- On- or Off-Chip Reference Oscillator Operation
- Single Modulus 4-Bit Data Bus Programming
- ÷N Range = 4 to 4092 in Steps of Eight
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Pin-for-Pin Compatible with the MN6044

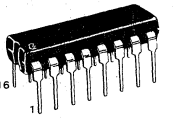
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

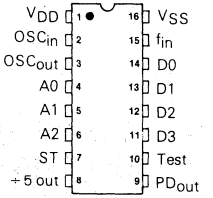


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGNS
PRODUCT BEING PHASED OUT

Closest equivalent is the MC145145-1

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MOTOROLA

MC145145-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

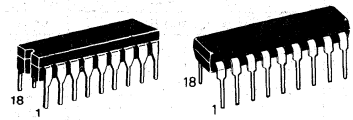
4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145145-1 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145145-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145145-1.

The MC145145-1 offers improved performance over the MC145145. The ac characteristics have been improved and the input current requirements have been modified.

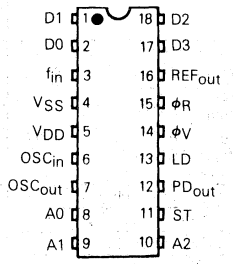
- General Purpose Applications:
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two Way Radios — Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Single Modulus 4-Bit Data Bus Programming
- ÷ R Range = 3 to 4095
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  Single Ended (Three State)
  Double Ended



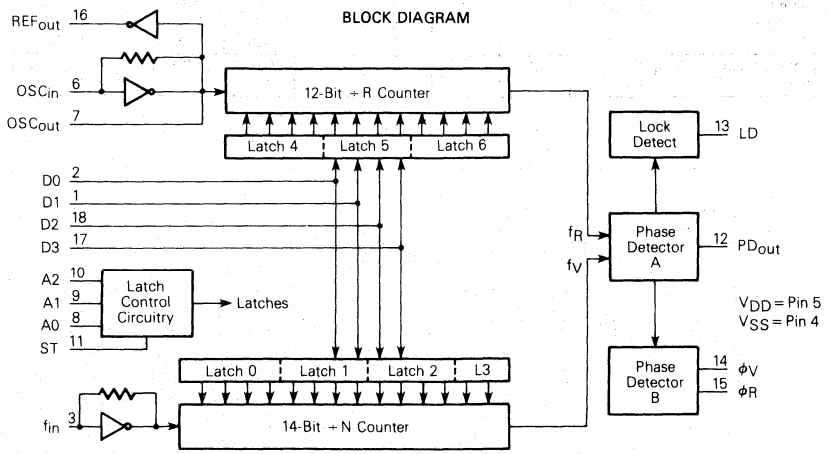
MC145145L1
CERAMIC PACKAGE
CASE 726

MC145145P1
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level V_{in}=0 V or V_{DD} I_{out}≈0 μA	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
		5	–	0.05	–	0.001	0.05	–	0.05	
		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level V_{out}=0.5 V or V_{DD}−0.5 V (All Outputs Except OSC_{out})	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
		5	–	1.5	–	2.25	1.5	–	1.5	
		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current V_{out}=2.7 V Source	I_{OH}	3	−0.44	–	−0.35	−1.0	–	−0.22	–	mA
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Other Inputs	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 μA	I_{DD}	3	–	800	–	200	800	–	1600	μA
		5	–	1200	–	300	1200	–	2400	
		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current – PD_{out} V_{out}=0 V or 9 V	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA

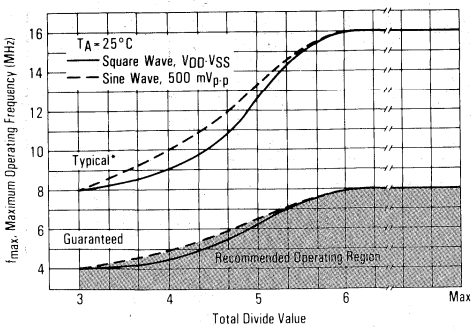
SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time (Figures 1 and 6)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Setup Times	t_{su}	3	10	0	–	ns
Data to ST (Figure 2)		5	10	0	–	
		9	10	0	–	
Address to ST (Figure 2)		3	80	60	–	
		5	50	30	–	
		9	30	18	–	
Hold Times	t_h	3	25	10	–	ns
Data to Strobe (Figure 2)		5	20	10	–	
		9	15	10	–	
Address to Strobe (Figure 2)		3	35	15	–	
		5	25	10	–	
		9	20	10	–	
Output Pulse Width	$t_{w\phi}$	3	25	100	175	ns
ϕ_R, ϕ_V with f_R in		5	20	60	100	
Phase with f_V (Figures 3 and 6)		9	10	40	70	
Input Rise and Fall Times	t_r, t_f	3	–	20	5	μs
OSC_{in}, f_{in} (Figure 4)		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width	t_w	3	40	30	–	ns
ST (Figure 5)		5	35	20	–	
		9	25	15	–	

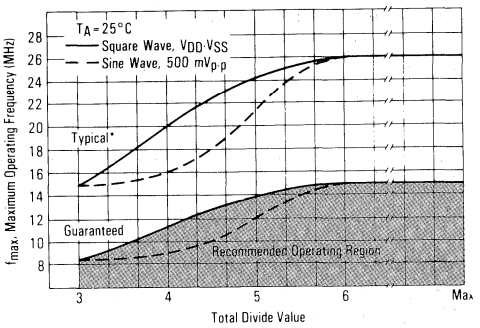
6

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

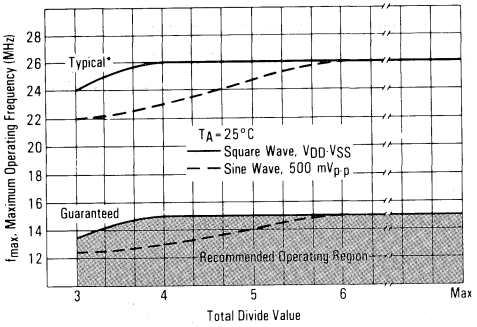
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

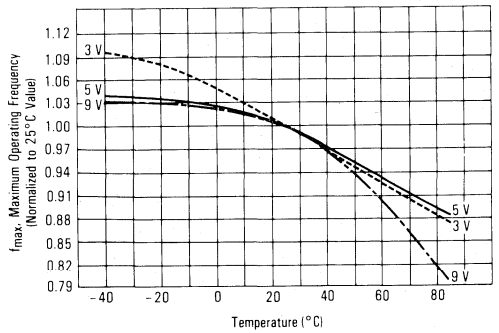


GRAPH 1C — V_{DD} = 9 V

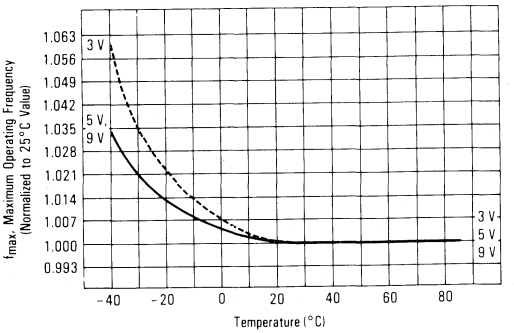


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

DATA INPUTS (Pins 2, 1, 18, 17) – Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 17 (D3) is most significant.

f_{in} (Pin 3) – Input to ÷N portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels) DC coupling may be used.

V_{SS} (Pin 4) – Circuit Ground.

V_{DD} (Pin 5) – Positive power supply.

OSC_{in}, OSC_{out} (Pins 6 and 7) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 8, 9, 10) – A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷N Bits	0	1	2	3
0	0	1	Latch 1	÷N Bits	4	5	6	7
0	1	0	Latch 2	÷N Bits	8	9	10	11
0	1	1	Latch 3	÷N Bits	12	13	–	–
1	0	0	Latch 4	Reference Bits	0	1	2	3
1	0	1	Latch 5	Reference Bits	4	5	6	7
1	1	0	Latch 6	Reference Bits	8	9	10	11
1	1	1	–	–	–	–	–	–

ST (Pin 11) – When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low, will latch that information. When high, any changes in the data information will be transferred into the latches.

PD_{out} (Pin 12) – Three-state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses.
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses.
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

LD (Pin 13) – Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

ϕV, ϕR (Pins 14 and 15) – These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frquency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

REF_{out} (Pin 16) – Buffered output of on-chip reference oscillator or externally provided reference-input signal.

SWITCHING WAVEFORMS

FIGURE 1

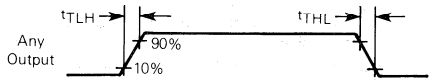


FIGURE 2

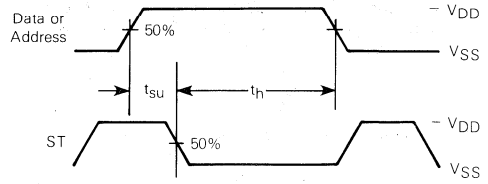
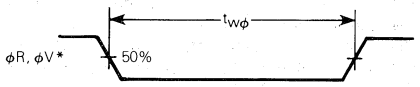


FIGURE 3



* f_r in phase with f_v

FIGURE 4

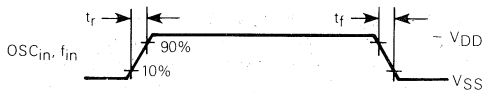


FIGURE 5

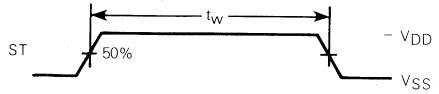
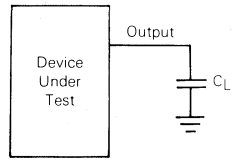
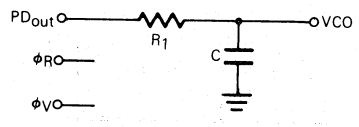


FIGURE 6 — TEST CIRCUIT



PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

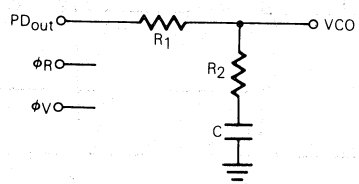


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

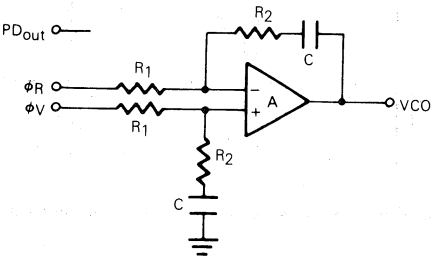


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

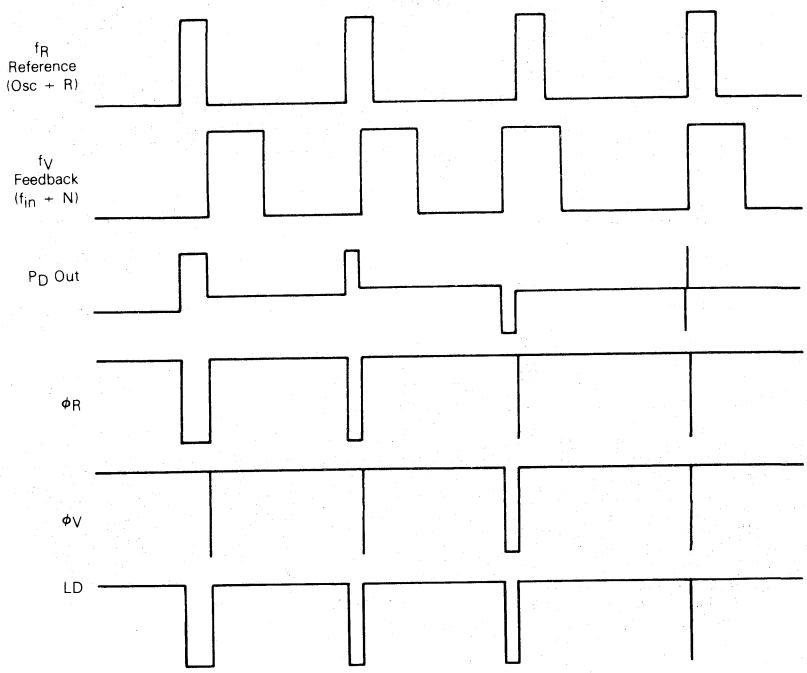
for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input),

$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

FIGURE 7 — PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

APPLICATIONS

The features of the MC145145-1 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor-controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The ÷ R programmability is used to advantage in Figure 8. Here, the nominal ÷ R value is 3667; but by programming small changes in this value, fine tuning is accomplished. Better tuning resolution is achievable with this method than by changing the ÷ N, due to the use of the large fixed prescaling value of ÷ 256 provided by the MC12071.

The two loop synthesizer, in Figure 9, takes advantage of these features to control the phase locked loop with a minimum of dedicated lines while preserving optimal loop performance. Both 25 Hz and 100 Hz steps are provided while the relatively large reference frequencies of 10 kHz or 10.1 kHz are maintained.

FIGURE 8 — TV/CATV TUNING SYSTEM

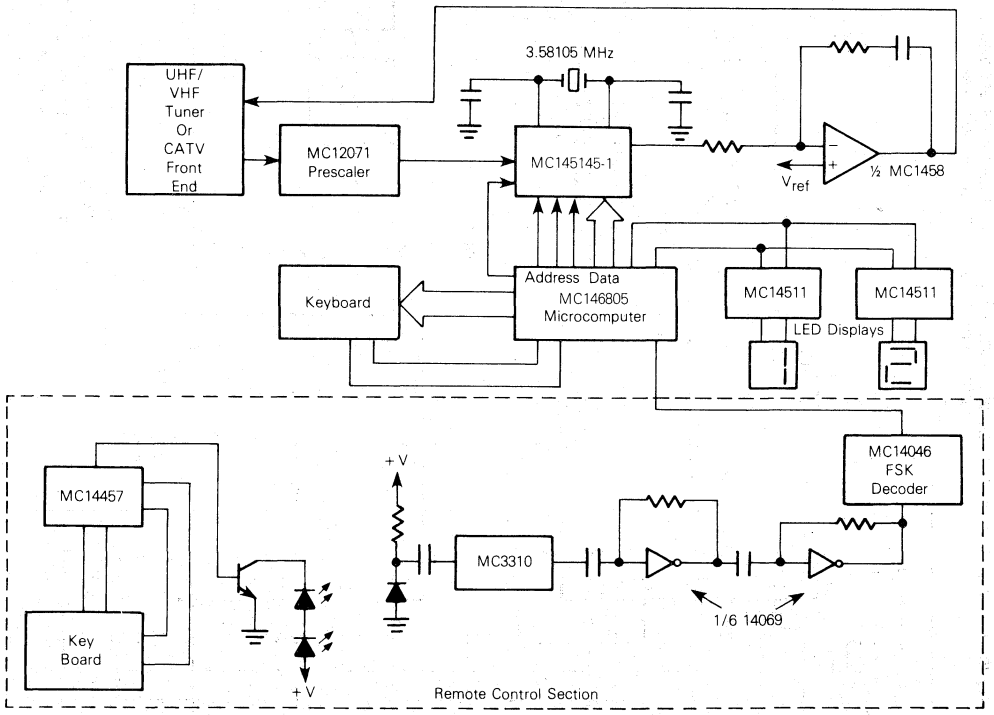


FIGURE 9 — TWO-LOOP SYNTHESIZER PROVIDES 25 AND 100 Hz FREQUENCY STEPS WHILE MAINTAINING HIGH DETECTOR COMPARISON FREQUENCIES OF 10 AND 10.1 kHz

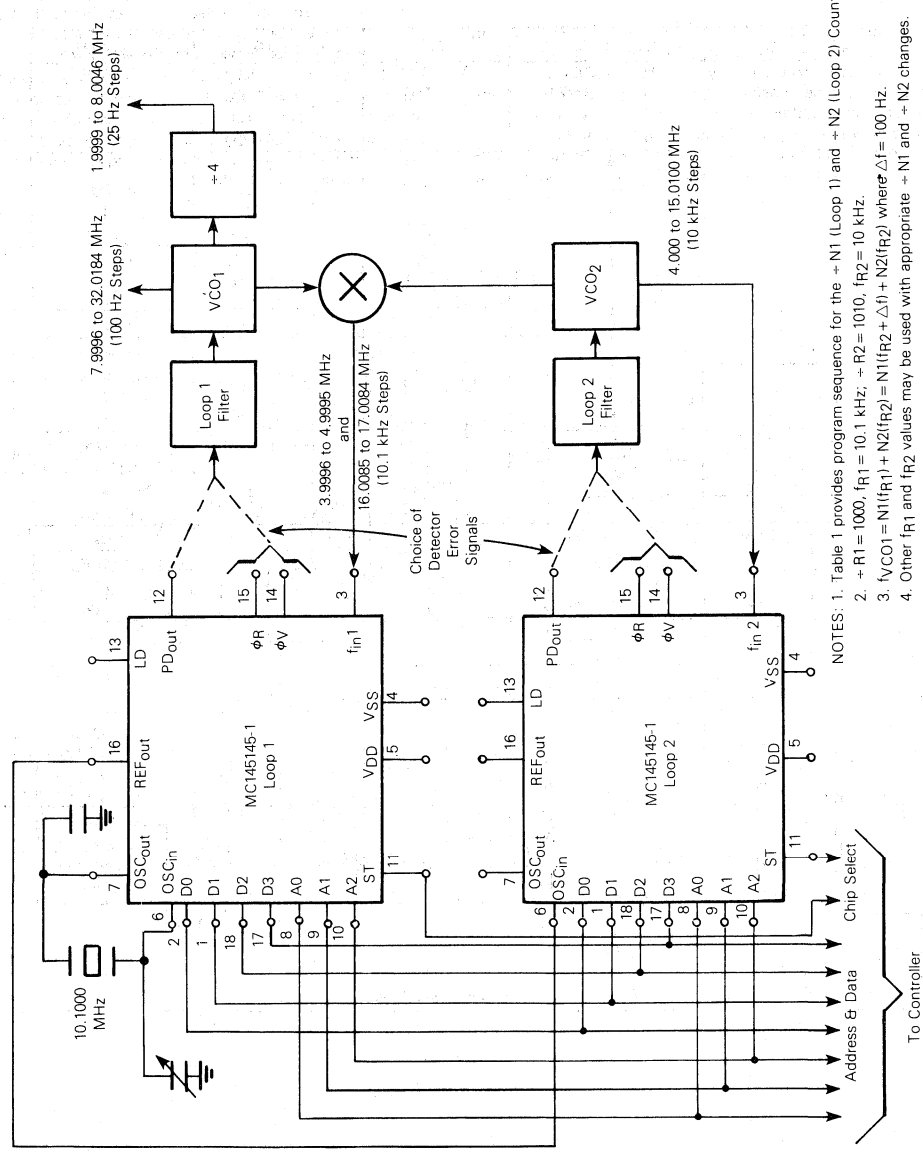


TABLE 1 — PROGRAMMING SEQUENCE FOR TWO-LOOP SYNTHESIZER OF FIGURE 9

÷N1	f_{in1} (MHz)	÷N2	f_{VCO2} (MHz)	f_{VCO1} (MHz)
396 "A" 397 495	3.9996 "B" 4.0097 4.9995	400 399 301	4.0000 3.9900 3.0100	7.9996 7.9997 8.0095
"A"	"B"	401 400 302	4.0100 4.0000 3.0200	8.0096 8.0097 8.0195
"A"	"B"	402 "C" 401 303	4.0200 "D" 4.0100 3.0300	8.0196 8.0197 8.0295
		1500	15.0000	Increasing In 100 Hz Steps 19.9995
"A"	"B"	1600 1599 1501	16.0000 15.9900 15.0100	19.9996 19.9997 20.0095
1585 "E" 1586 1684	16.0085 "F" 16.0186 17.0084			20.0085 20.0086 20.0184
"E"	"F"	"C"	"D"	20.0185 20.0186 20.0284
				Increasing In 100 Hz Steps 32.0084
"E"	"F"			32.0085 32.0086 32.0184

6

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L=\frac{C_{in}C_{out}}{C_{in}+C_{out}}+C_a+C_O+\frac{C1\cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

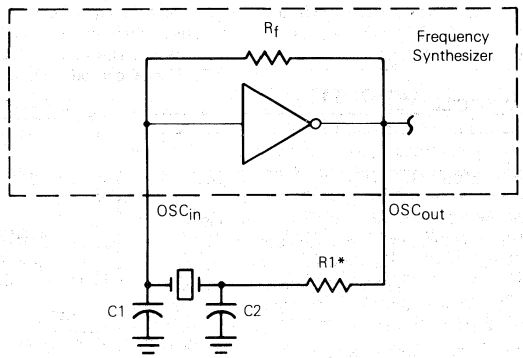
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

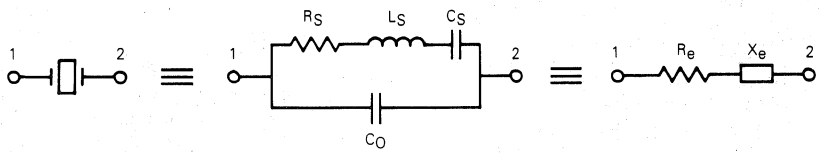
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



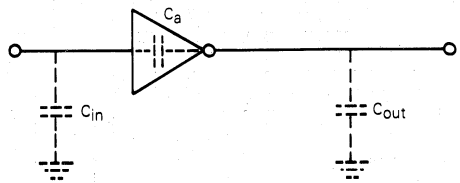
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES OF THE AMPLIFIER



6

MOTOROLA

MC145146-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

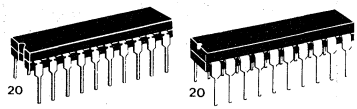
4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145146-1 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital phase detector, 10-bit programmable divide-by-N counter, 7-bit divide-by-A counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145146-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and the MC145146-1.

The MC145146-1 offers improved performance over the MC145146. Modulus Control output drive has been increased and the ac characteristics have been improved. The input current requirements have also been modified.

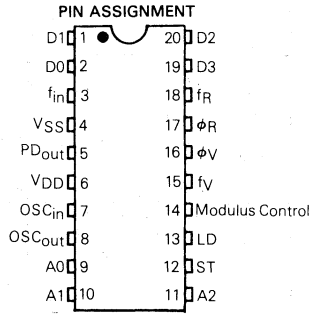
- General Purpose Applications:
  - CATV
  - AM/FM Radios
  - Two Way Radios
  - TV Tuning
  - Scanning Receivers
  - Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Dual Modulus 4-Bit Data Bus Programming
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single Ended (Three State)
  - Double Ended
- Chip Complexity: 5692 FETs or 1423 Equivalent Gates

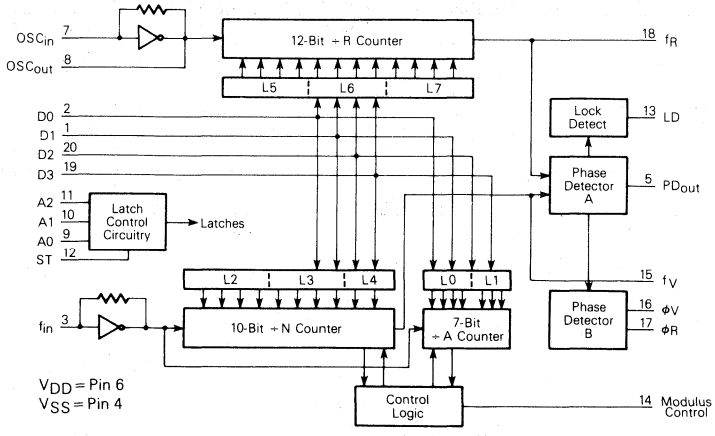


MC145146L1
CERAMIC PACKAGE
CASE 732

MC145146P1
PLASTIC PACKAGE
CASE 738

PIN ASSIGNMENT





This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
V_{in}=0 V or V_{DD}		5	–	0.05	–	0.001	0.05	–	0.05	
I_{out}≈0 μA		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
V_{out}=0.5 V or V_{DD}−0.5 V		5	–	1.5	–	2.25	1.5	–	1.5	
(All Outputs Except OSC_{out})		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – Modulus Control	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.60	–	−0.50	−1.5	–	−0.30	–	
V_{out}=4.6 V		5	−0.90	–	−0.75	−2.0	–	−0.50	–	
V_{out}=8.5 V		9	−1.50	–	−1.25	−3.2	–	−0.80	–	
V_{out}=0.3 V Sink	I_{OL}	3	1.30	–	1.10	5.0	–	0.66	–	
V_{out}=0.4 V		5	1.90	–	1.70	6.0	–	1.08	–	
V_{out}=0.5 V		9	3.80	–	3.30	10.0	–	2.10	–	
Output Current – Other Outputs	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Other Inputs	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	μA
V_{in}=0 V or V_{DD}		5	–	1200	–	300	1200	–	2400	
I_{out}=0 μA		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current – PD_{out}	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA
V_{out}=0 V or 9 V										

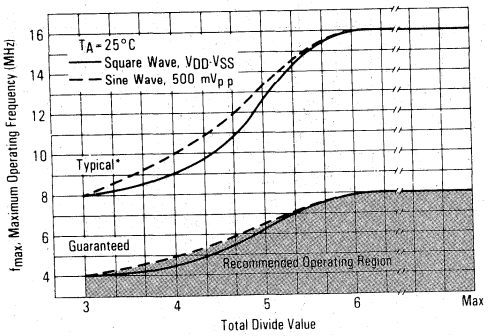
6

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

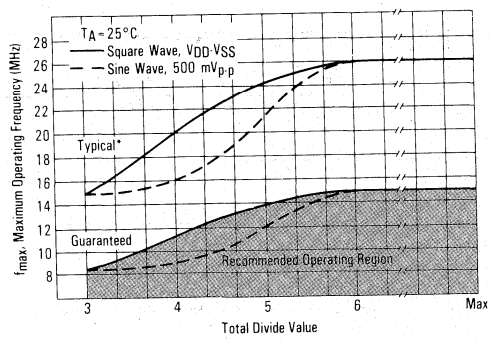
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 1 and 7)	t_{TLH}	3	–	50	115	ns
		5	–	30	60	
		9	–	20	40	
Output Fall Time, Modulus Control (Figures 1 and 7)	t_{THL}	3	–	25	60	ns
		5	–	17	34	
		9	–	15	30	
Output Rise and Fall Time, Other Outputs (Figure 1)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 2 and 7)	t_{PLH}, t_{PHL}	3	–	55	125	ns
		5	–	40	80	
		9	–	25	50	
Setup Times	t_{su}					ns
Data to ST (Figure 3)		3	10	0	–	
		5	10	0	–	
		9	10	0	–	
Address to ST (Figure 3)		3	80	60	–	
		5	50	30	–	
		9	30	18	–	
Hold Times	t_h					ns
Address to ST (Figure 3)		3	35	15	–	
		5	25	10	–	
		9	20	10	–	
Data to Strobe (Figure 3)		3	25	10	–	
		5	20	10	–	
		9	15	10	–	
Output Pulse Width, ϕ_R, ϕ_V with f_r in Phase with f_V (Figures 4 and 7)	$t_{w\phi}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times OSC_{in}, f_{in}, ST (Figure 5)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width ST, (Figure 6)	t_w	3	40	30	–	ns
		5	35	20	–	
		9	25	15	–	

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

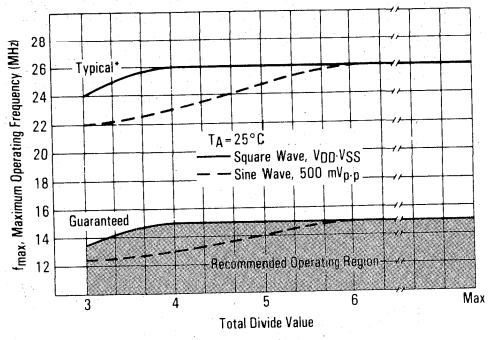
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

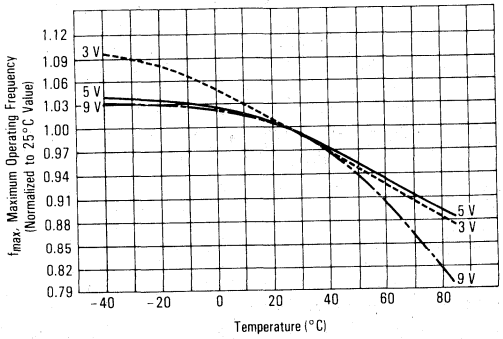


GRAPH 1C — V_{DD} = 9 V

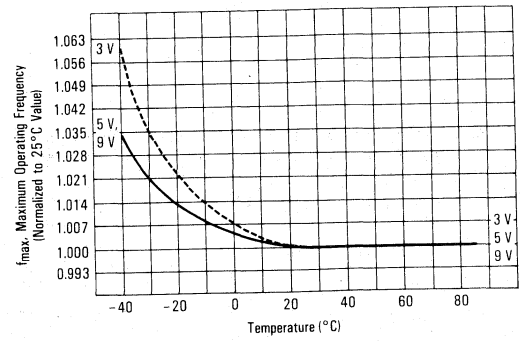


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6

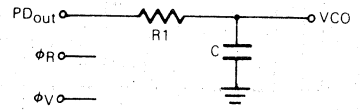


*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

6

PHASE LOCKED LOOP — LOW-PASS FILTER DESIGN

A)

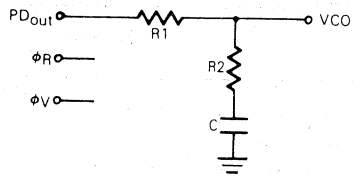


$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NR1C}}$$

$$\zeta = 0.5\omega_N (N/K_\phi K_{VCO})$$

$$F(s) = \frac{1}{R1CS + 1}$$

B)

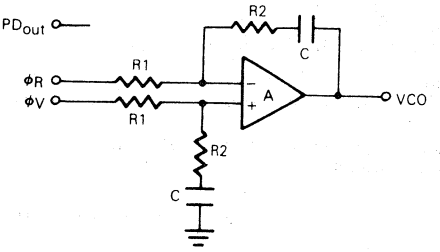


$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NC(R1 + R2)}}$$

$$\zeta = 0.5\omega_N (R2C + N/K_\phi K_{VCO})$$

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

C)



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NCR1}}$$

$$\zeta = \frac{\omega_N R2C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R2CS + 1}{R1CS}$$

NOTE: Sometimes R1 is split into two series resistors each R1 ÷ 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

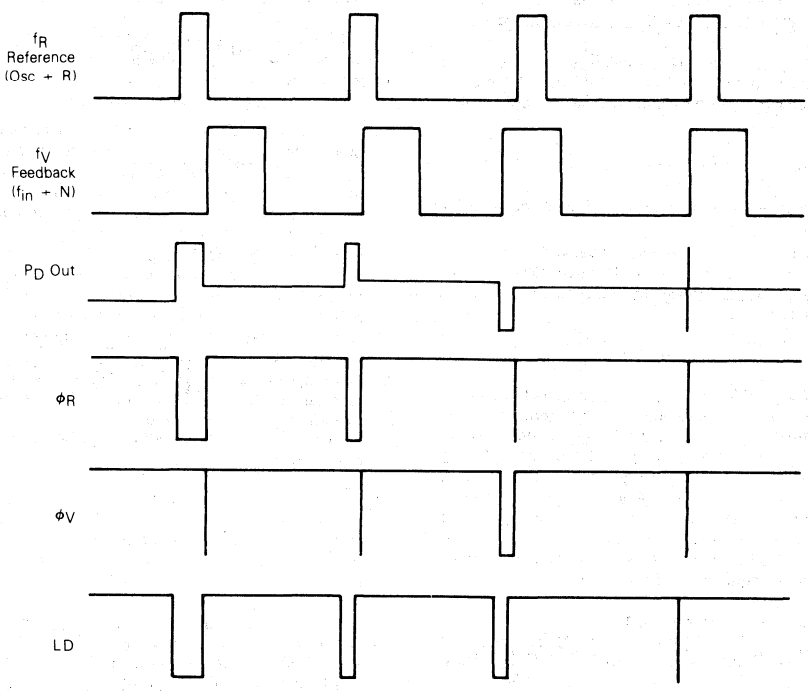
$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N \cong (2\pi/10)\, f_r$ (at phase detector input)

$\zeta \cong 1$

FIGURE 8
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

PIN DESCRIPTIONS

DATA INPUTS (Pins 2, 1, 20, 19) – Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 19 (D3) is most significant.

f_{in} (Pin 3) – Input to ÷N portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels), DC coupling may be used.

V_{SS} (Pin 4) – Circuit Ground.

PD_{out} (Pin 5) – Three-state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses.
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses.
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

V_{DD} (Pin 6) – Positive power supply.

OSC_{in}, OSC_{out} (Pins 7 and 8) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 9, 10, 11) – A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷A Bits	0	1	2	3
0	0	1	Latch 1	÷A Bits	4	5	6	–
0	1	0	Latch 2	÷N Bits	0	1	2	3
0	1	1	Latch 3	÷N Bits	4	5	6	7
1	0	0	Latch 4	÷N Bits	8	9	–	–
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST (Pin 12) – When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low, will latch that information. When high, any changes in the data information will be transferred into the latches.

LD (Pin 13) – Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

MODULUS CONTROL (Pin 14) – Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N-A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the ÷A counter.

f_V (Pin 15) – This is the output of the ÷N counter that is internally connected to the phase detector input. With this output available, the ÷N counter can be used independently.

ϕ_V, ϕ_R (Pins 16 and 17) – These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frquency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R (Pin 18) – This is the output of the ÷R counter that is internally connected to the phase detector input. With this output available, the ÷R counter can be used independently.

SWITCHING WAVEFORMS

FIGURE 1

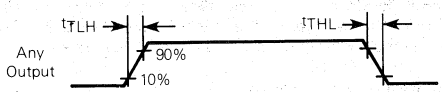


FIGURE 2

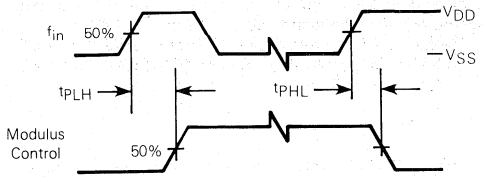


FIGURE 3

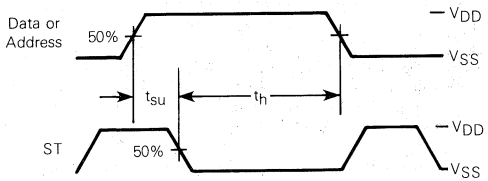
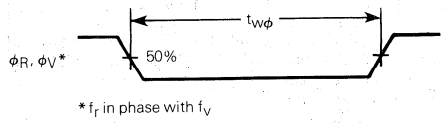


FIGURE 4



* f_r in phase with f_v

FIGURE 5

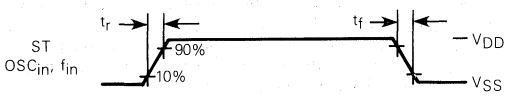


FIGURE 6

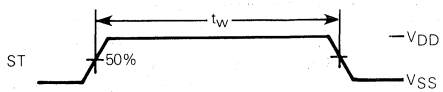
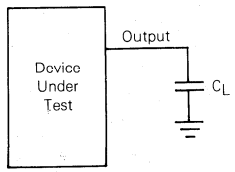


FIGURE 7 — TEST CIRCUIT

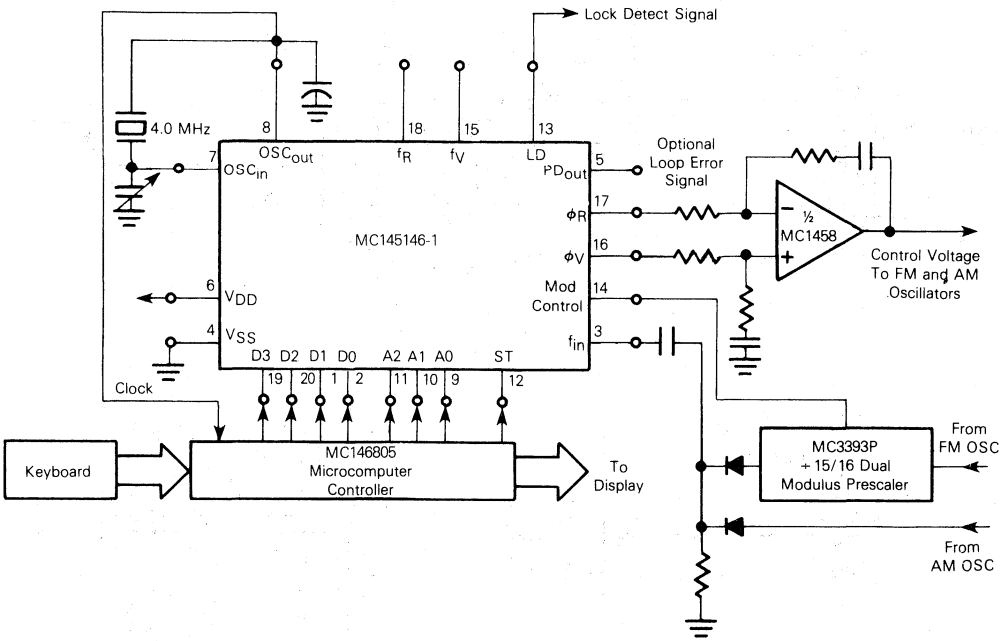


APPLICATIONS

The features of the MC145146-1 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

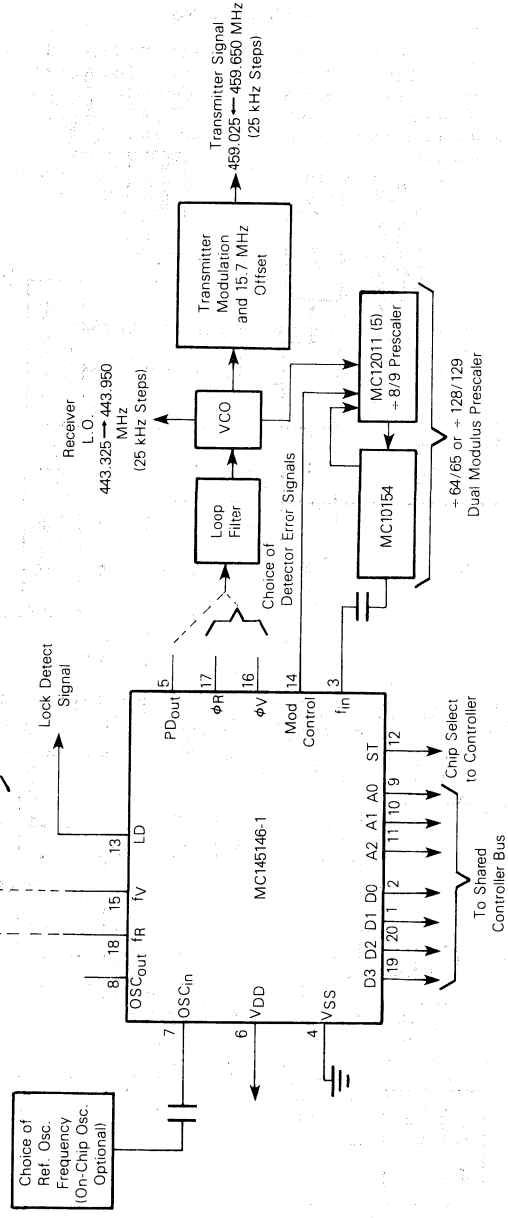
The device architecture allows the user to establish any integer reference divide value between 3 and 4095. The wide selection of ÷R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a microprocessor system clock. Typical applications that take advantage of these MC145146-1 features including the dual modulus capability are shown in Figures 9, 10, and 11.

FIGURE 9 — FM/AM BROADCAST RADIO SYNTHESIZER



NOTES: 1) For FM: Channel spacing = f_R = 25 kHz, ÷R = 160.
For AM: Channel spacing = f_R = 1 kHz, ÷R = 4000.
2) Various channel spacings and reference oscillator frequencies can be chosen since any ÷R value from 3 to 4095 can be established.
3) Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.

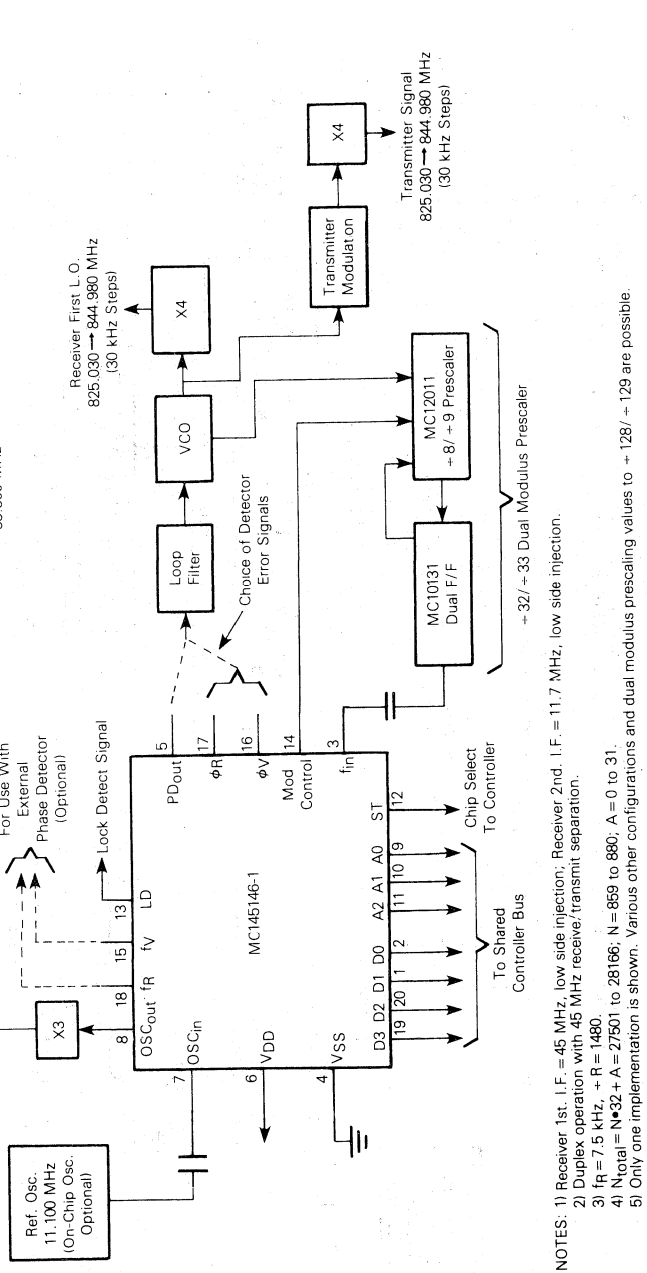
FIGURE 10 — SYNTHESIZER FOR UHF MOBILE RADIO TELEPHONE CHANNELS DEMONSTRATES USE OF THE MC145146-1 IN MICROPROCESSOR/MICROCOMPUTER CONTROLLED SYSTEMS OPERATING TO SEVERAL HUNDRED MHz



NOTES: 1) Receiver I.F. = 10.7 MHz, low side injection.
2) Duplex operation with 5 MHz receive/transmit separation.
3) f_R = 25 kHz, ÷R chosen to correspond with desired reference oscillator frequency.
4) N_{total} = 17733 to 17758 = N•P + A; N = 277, A = 5 to 30 for P = 64.
5) For faster response, use the MC10154 down counter.

6

FIGURE 11 — 666 CHANNEL, COMPUTER CONTROLLED, MOBILE RADIO TELEPHONE SYNTHESIZER FOR 800 MHz CELLULAR RADIO SYSTEMS



NOTES: 1) Receiver 1st. I.F. = 45 MHz, low side injection; Receiver 2nd. I.F. = 11.7 MHz, low side injection.
2) Duplex operation with 45 MHz receive/transmit separation.
3) f_R = 7.5 kHz, ÷ R = 1480.
4) Ntotal = N•32 + A = 27501 to 28166; N = 859 to 880; A = 0 to 31.
5) Only one implementation is shown. Various other configurations and dual modulus prescaling values to ÷ 128/÷ 129 are possible.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L=\frac{C_{in}C_{out}}{C_{in}+C_{out}}+C_a+C_O+\frac{C1\cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

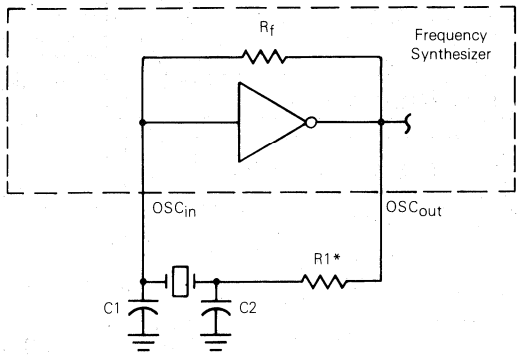
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

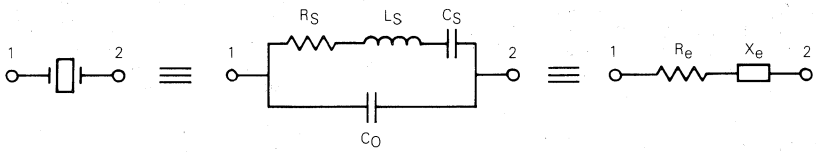
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



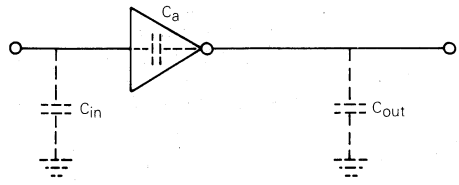
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES OF THE AMPLIFIER



MOTOROLA

MC145151-1

Advance Information

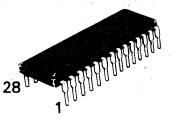
HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE
PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

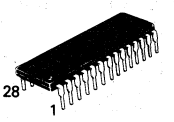
The MC145151-1 is programmed by 14 parallel input-data lines. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector and 14-bit programmable divide-by-N counter. When combined with a loop filter and VCO, the MC145151-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145151-1.

The MC145151-1 offers improved performance over the MC145151. The ac characteristics have been improved and the input current requirements have been modified.

- General Purpose Applications:
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values — 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  Single Ended (Three-State)
  Double Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

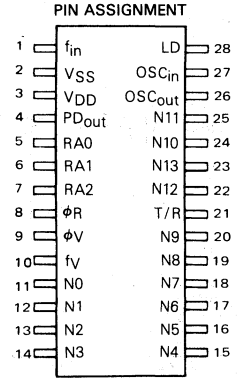


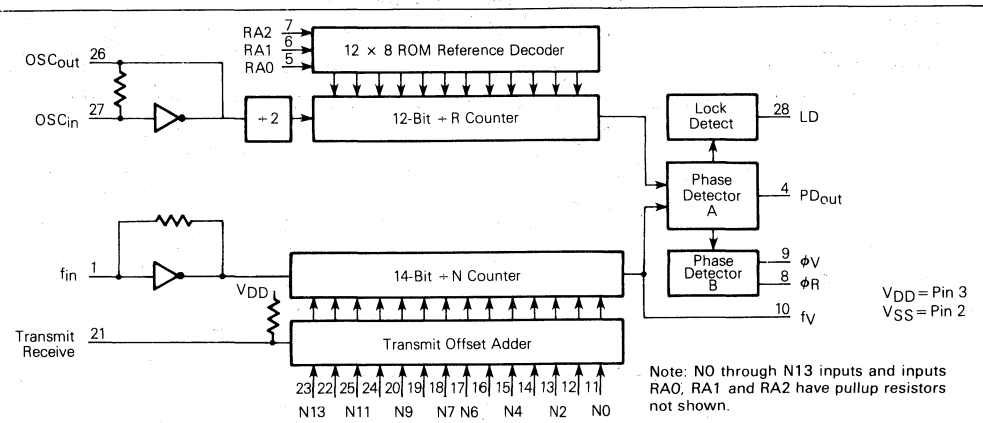
MC145151L1
CERAMIC PACKAGE
CASE 733



MC145151P1
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT





Note: N0 through N13 inputs and inputs RA0, RA1 and RA2 have pullup resistors not shown.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level V_{in}=0 V or V_{DD} I_{out}≈0 μA	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
		5	–	0.05	–	0.001	0.05	–	0.05	
		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level V_{out}=0.5 V or V_{DD}−0.5 V (All Outputs Except OSC_{out})	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
		5	–	1.5	–	2.25	1.5	–	1.5	
		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current V_{out}=2.7 V Source	I_{OH}	3	−0.44	–	−0.35	−1.0	–	−0.22	–	mA
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current − f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Current − Other Inputs (with Pullups)	I_{IH}	9	–	0.3	–	0.00001	0.1	–	1.0	μA
	I_{IL}	9	–	−400	–	−90	−200	–	−170	
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance − PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 μA	I_{DD}	3	–	800	–	200	800	–	1600	μA
		5	–	1200	–	300	1200	–	2400	
		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current − PD_{out} V_{out}=0 V or 9 V	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA

6

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time (Figures 1 and 4)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Output Pulse Width, ϕR, ϕV with f_R in Phase with f_V (Figures 2 and 4)	$t_{w(\phi)}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times OSC_{in}, f_{in} (Figure 3)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	

PIN DESCRIPTIONS

f_{in} (Pin 1) – Input to ÷ N portion of synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into Pin 9. For larger amplitude signals (standard CMOS Logic levels) dc coupling may be used.

V_{SS} (Pin 2) – Circuit ground.

V_{DD} (Pin 3) – Positive power supply.

PD_{out} (Pin 4) – Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

RA0, RA1, RA2 (Pins 5, 6, and 7) – These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

ϕR, ϕV (Pins 8 and 9) – These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

f_V (Pin 10) – This is the output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

N Inputs (Pins 11 to 20 and 22 to 25) – These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is least significant and N13 is most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Transmit/Receive (Pin 21) – This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pullup resistor ensures that no connection will appear as a logic one causing no offset addition.

OSC_{out}, OSC_{in} (Pins 26 and 27) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal will typically be ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

LD (Pin 28) – Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

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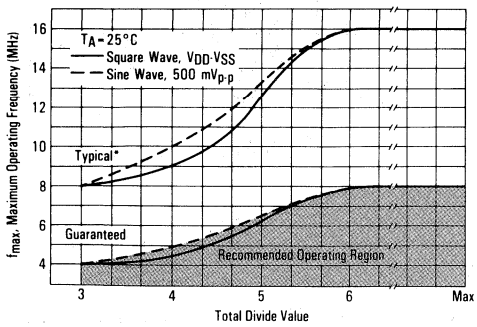
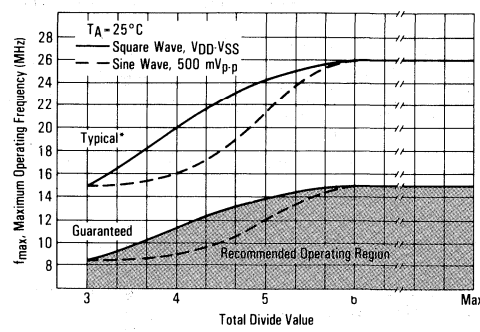
GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

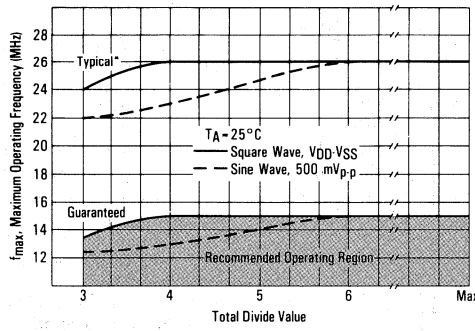
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

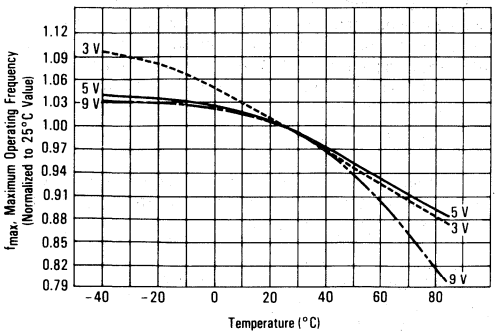


GRAPH 1C — V_{DD} = 9 V

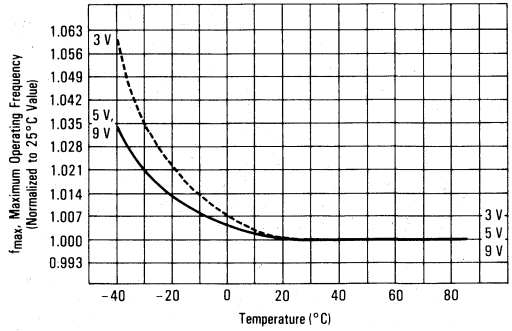


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



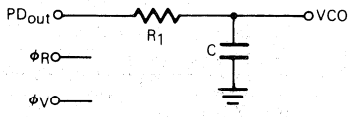
GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

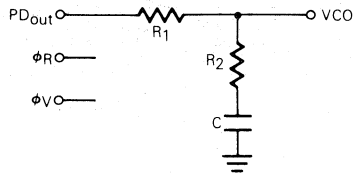


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

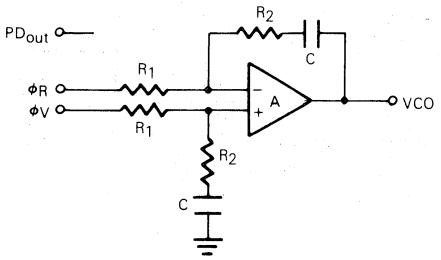


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input),

$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

SWITCHING WAVEFORMS

FIGURE 1

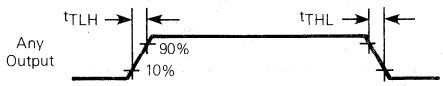
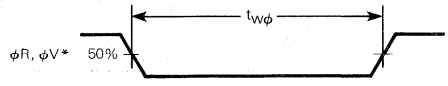


FIGURE 2



* f_r in phase with f_v

FIGURE 3

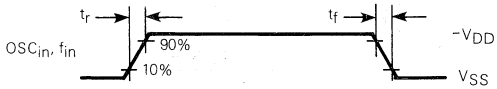
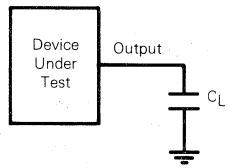
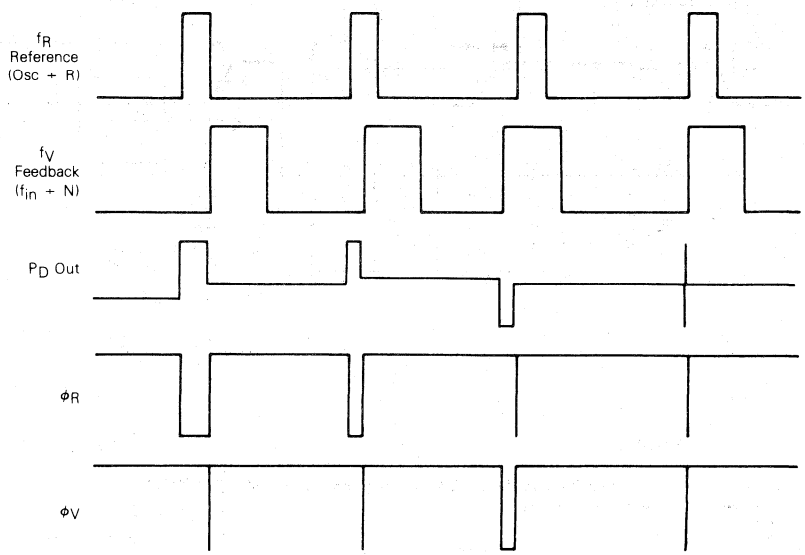


FIGURE 4 -- TEST CIRCUIT



6

FIGURE 5
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

FIGURE 6 — 5 MHz TO 5.5 MHz LOCAL OSCILLATOR CHANNEL SPACING = 1 kHz

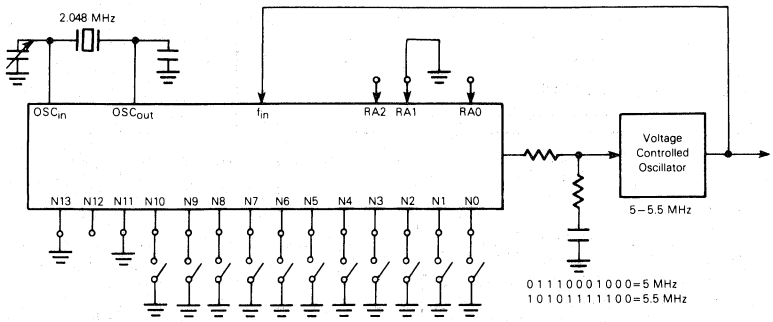
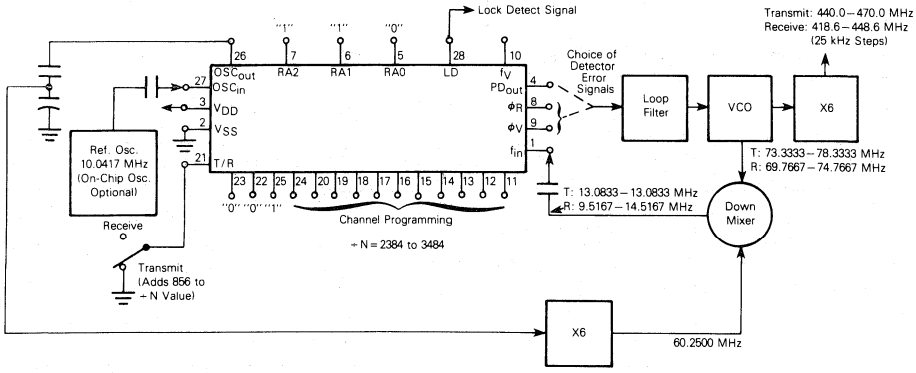


FIGURE 7 — SYNTHESIZER FOR LAND MOBILE RADIO UHF BANDS



NOTES:
1) $f_R = 4.1667$ kHz; ÷R = 2410; 21.4 MHz low side injection during receive
2) MC145151-1 current drain ≅ 5 mA for $V_{DD} = 5$ Vdc
3) Frequency values shown are for the 440–470 MHz band. Similar implementation applies to the 406–441 MHz band. For 470–512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz)

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD} = 5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

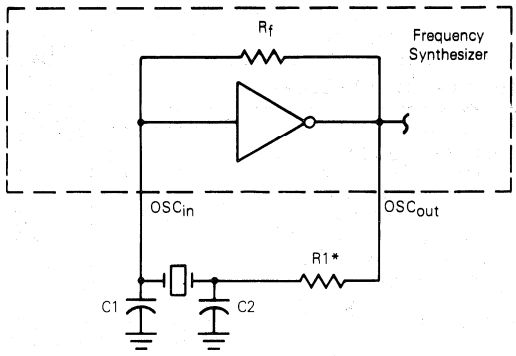
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

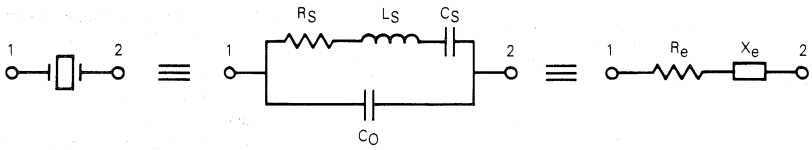
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



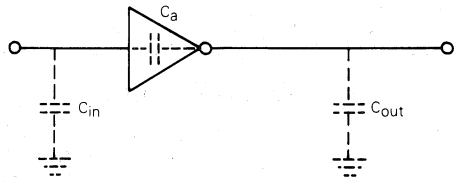
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES
OF THE AMPLIFIER



MOTOROLA

MC145152-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

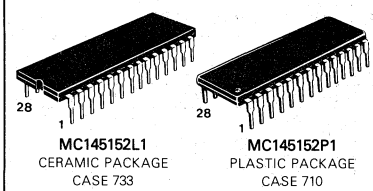
PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

The MC145152-1 is programmed by sixteen parallel inputs. The device features consist of a reference oscillator, selectable-reference divider, two output phase dectector, 10-bit programmable divide-by-N counter and 6-bit programmable ÷ A counter. When combined with a loop filter and VCO, the MC145152-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145152-1.

The MC145152-1 offers improved performance over the MC145152. Modulus Control output drive has been increased and the ac characteristics have been improved. Input current requirements have also been changed.

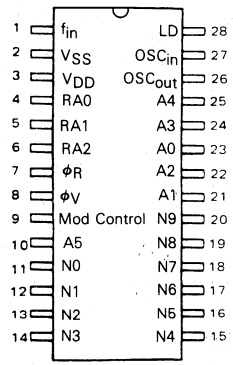
- General Purpose Applications:
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values — 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



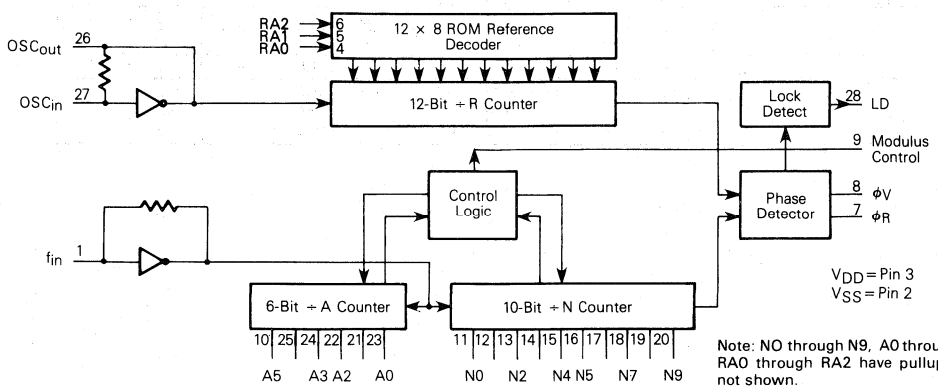
MC145152L1
CERAMIC PACKAGE
CASE 733

MC145152P1
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



BLOCK DIAGRAM



Note: NO through N9, A0 through A5 and RA0 through RA2 have pullup resistors not shown.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

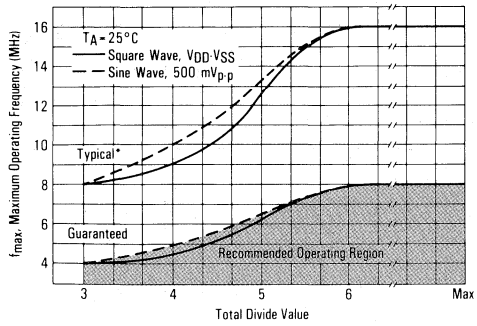
Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
V_{in}=0 V or V_{DD}		5	–	0.05	–	0.001	0.05	–	0.05	
I_{out}≈0 μA		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
V_{out}=0.5 V or V_{DD}−0.5 V		5	–	1.5	–	2.25	1.5	–	1.5	
(All Outputs Except OSC_{out})		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – Modulus Control	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.60	–	−0.50	−1.5	–	−0.30	–	
V_{out}=4.6 V		5	−0.90	–	−0.75	−2.0	–	−0.50	–	
V_{out}=8.5 V		9	−1.50	–	−1.25	−3.2	–	−0.80	–	
V_{out}=0.3 V Sink	I_{OL}	3	1.30	–	1.10	5.0	–	0.66	–	
V_{out}=0.4 V		5	1.90	–	1.70	6.0	–	1.08	–	
V_{out}=0.5 V		9	3.80	–	3.30	10.0	–	2.10	–	
Output Current – Other Outputs	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Current – Other Inputs	I_{IH}	9	–	0.3	–	0.00001	0.1	–	1.0	μA
(with Pullups)	I_{IL}	9	–	−400	–	−90	−200	–	−170	
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	μA
V_{in}=0 V or V_{DD}		5	–	1200	–	300	1200	–	2400	
I_{out}=0 μA		9	–	1600	–	400	1600	–	3200	

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

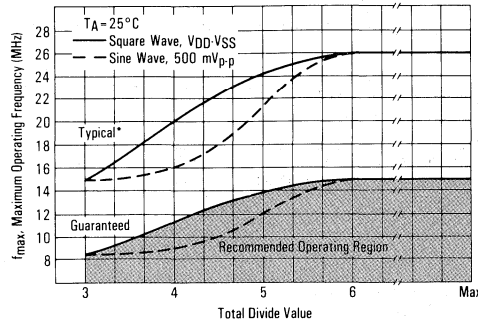
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 1 and 5)	t_{TLH}	3	–	50	115	ns
		5	–	30	60	
		9	–	20	40	
Output Fall Time, Modulus Control (Figures 1 and 5)	t_{THL}	3	–	25	60	ns
		5	–	17	34	
		9	–	15	30	
Output Rise and Fall Time, LD, ϕV, ϕR (Figures 1 and 5)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 2 and 5)	t_{PLH}, t_{PHL}	3	–	55	125	ns
		5	–	40	80	
		9	–	25	50	
Output Pulse Width ϕR, ϕV with f_R in Phase With f_V (Figures 3 and 5)	$t_{W(\phi)}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times OSC_{in}, f_{in} (Figure 4)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

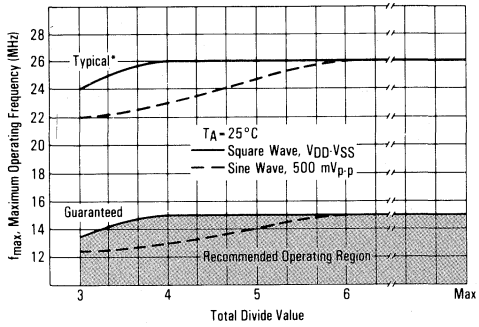
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

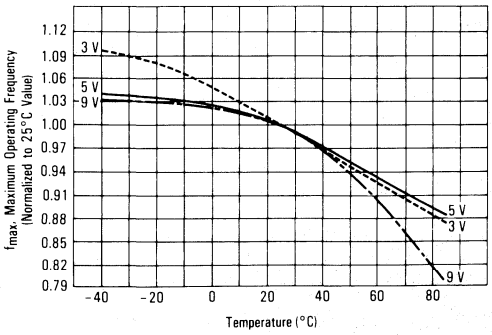


GRAPH 1C — V_{DD} = 9 V

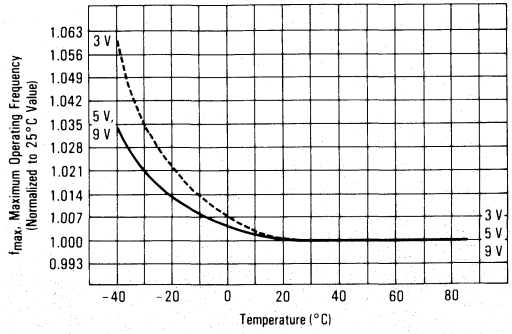


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

f_{in} (Pin 1) – Input to the positive edge triggered ÷N and ÷A counters. f_{in} is typically derived from a dual modulus prescaler and is AC coupled into Pin 1. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

V_{SS} (Pin 2) – Circuit Ground.

V_{DD} (Pin 3) – Positive power supply.

RA0, RA1, RA2 (Pins 4, 5, and 6) – These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

ϕ_R, ϕ_V (Pins 7 and 8) – These phase detector outputs can be combined externally for a loop error signal.

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency of f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MODULUS CONTROL (Pin 9) – Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the ÷A counter.

N INPUTS (Pins 11 through 20) – The N inputs provide the data that is preset into the ÷N counter when it reaches the count of zero. N0 is the least significant digit and N9 is the most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

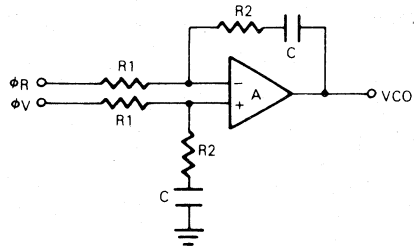
A INPUTS (Pins 23, 21, 22, 24, 25, 10) – The A inputs define the number of clock cycles of f_{in} that require a logic zero on the modulus control output. See page 8 for explanation of dual modulus prescaling. The A inputs all have internal pullup resistors that ensure that inputs left open will remain at a logic one.

OSC_{out}, OSC_{in} (Pins 26 and 27) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

LD (Pin 28) – Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

6

PHASE LOCKED LOOP – LOW PASS FILTER DESIGN



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NCR1}}$$

$$\zeta = \frac{\omega_N R2C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R2CS + 1}{R1CS}$$

NOTE. Sometimes R1 is split into two series resistors each R1 + 2 A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N.

DEFINITIONS: N = Total Division Ratio in feedback loop

$$K_\phi = V_{DD}/2\pi$$

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N \cong (2\pi/10)\, f_r$ (at phase detector input)

$\zeta \cong 1$

SWITCHING WAVEFORMS

FIGURE 1

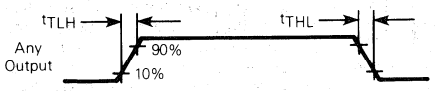


FIGURE 2

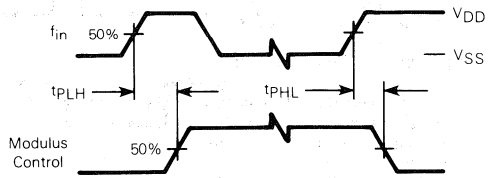
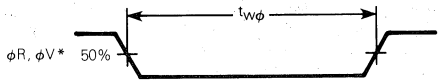


FIGURE 3



* f_r in phase with f_V

FIGURE 4

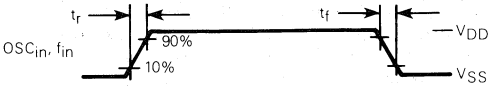


FIGURE 5 — TEST CIRCUIT

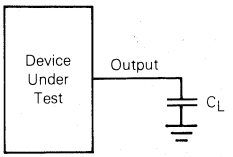
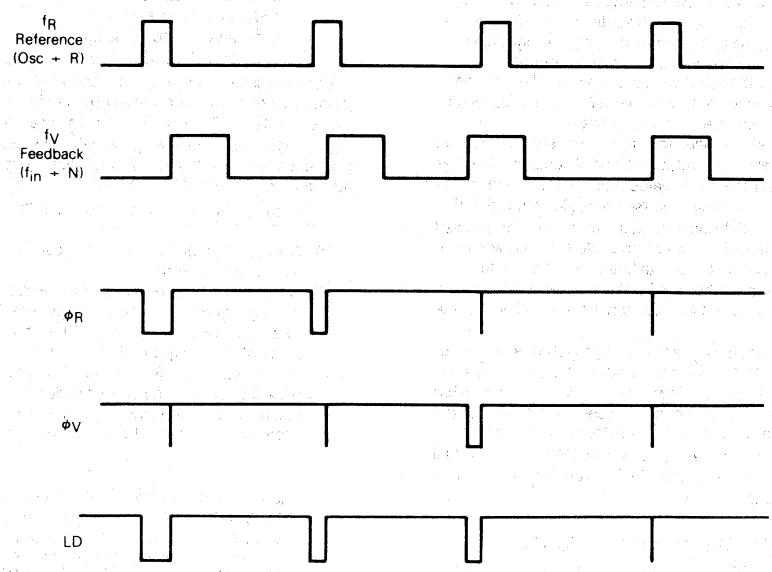


FIGURE 6
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is approximately equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

6

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145152-1 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷3/÷4 to ÷64/÷65 can be controlled by the MC145152-1.

Several dual modulus prescaler approaches suitable for use with the MC145152-1 are given in Figure 7. The approaches range from the low cost ÷15/÷16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145152-1 and dual modulus prescaling are shown in Figures 8 and 9 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145152-1

The system total divide value (N_{total}) will be dictated by the application. i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷N counter; A is the number programmed into the ÷A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P − 1 for a particular value N in the divide N counter. N is then incremented to N + 1 and the ÷A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the ÷N and ÷A counters. The constraint $N \geq A$ always applies. If $A_{max} = P - 1$ then $N_{min} \geq P - 1$. Then $N_{total-min} = (P-1)P + A$ or $(P-1)P$ since A is free to assume the value of zero.

$$N_{total-max} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of Pin 1 of the MC145152-1.

B. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the MC145152-1.

A sometimes useful simplification in the MC145152-1 programming code can be achieved by choosing the values for P of 8, 16, 32 or 64. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

A. Assume the ÷A counter contains "b" bits where $2^b = P$.

B. Always program all higher order ÷A counter bits above "b" to zero.

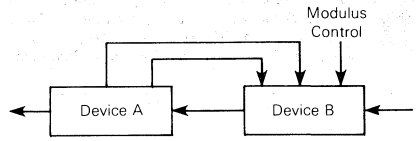
C. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10 + b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10 + b bit counter.

FIGURE 7 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145152-1

MC12009	÷5/÷6	440 MHz Min
MC12011	÷8/÷9	500 MHz Min
MC12013	÷10/÷11	500 MHz Min
MC12015	÷32/÷33	225 MHz Min
MC12016	÷40/÷41	225 MHz Min
MC12017	÷64/÷65	225 MHz Min
*MC12018	÷128/÷129	520 MHz Min
MC3393	÷15/÷16	140 MHz Typ

*Proposed introduction

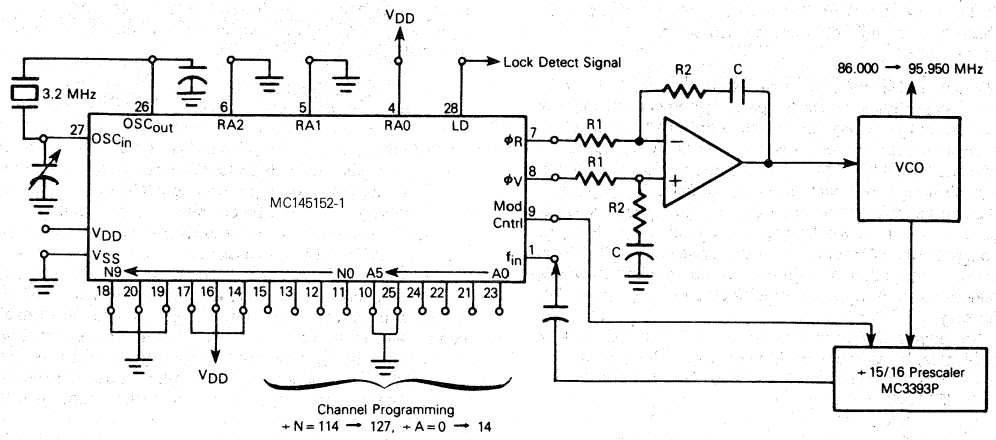
By using two devices, several dual modulus values are achievable:



Device A \ Device B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 or ÷80/÷81	÷64/÷65 or ÷128/÷129	÷80/÷81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

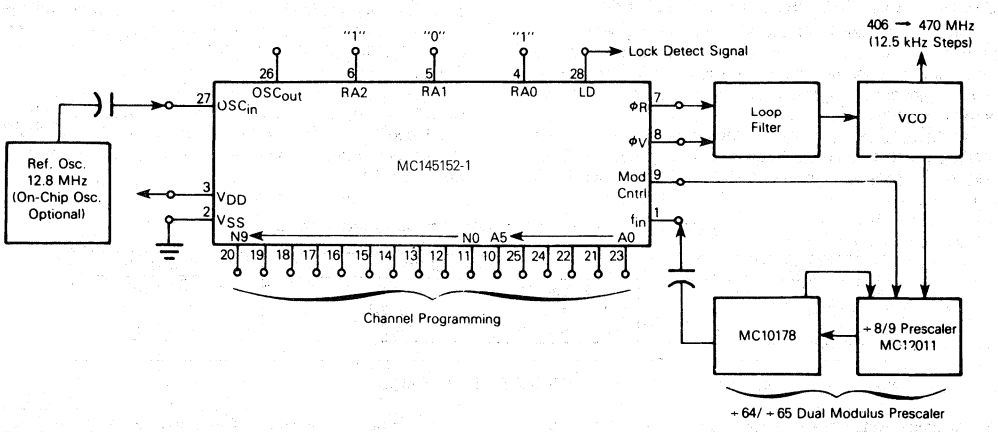
FIGURE 8 — AIRCRAFT NAV RECEIVER SYNTHESIZER DEMONSTRATES A LOW COST DUAL MODULUS SYSTEM EMPLOYING THE MC145152-1



NOTES:

1. $f_R = 50$ kHz, ÷ R = 64; 22.0 MHz low side injection; $N_{TOTAL} = 1720 \rightarrow 1919$.
2. Using 22.0 MHz for the receiver I.F. demonstrates how the choice of I.F. value can sometimes reduce the number of ÷ N bits that must be programmed. Using the more common 21.4 MHz I.F. would require six rather than four ÷ N programming inputs.

FIGURE 9 — SYNTHESIZER FOR LAND MOBILE RADIO UHF BAND COVERAGE DEMONSTRATES USE OF THE MC145152-1 IN SYSTEMS OPERATING TO SEVERAL HUNDRED MHz



NOTES:

1. $N_{TOTAL} = N \cdot 64 + A = 32480$ to 37600; N = 507 to 587, A = 0 to 63.
2. $f_R = 12.5$ kHz, ÷ R = 1024 (code 101).
3. The prescaling approach can be chosen for the application to enhance economy e.g., single chip MC3393P to approximately 100 MHz. MC12011 or MC12013 with dual flip flop to approximately 250 MHz. MC12011 or MC12013 with MC10178 to over 500 MHz.

6

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

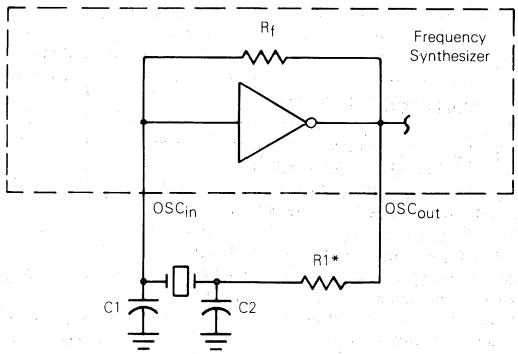
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

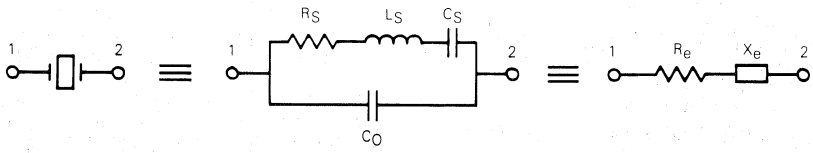
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



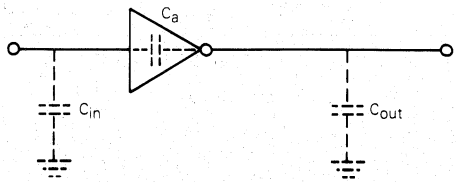
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES
OF THE AMPLIFIER



MOTOROLA

MC145155-1

Advance Information

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

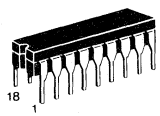
The MC145155-1 is programmed by a clocked, serial input, 16-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145155-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145155-1.

The MC145155-1 offers improved performance over the MC145155. The ac characteristics have been improved and the input current requirements have been modified.

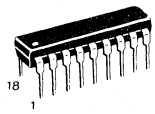
- General Purpose Applications:
  CATV, Two Way Radios, Scanning Receivers
  AM/FM Radios, TV Tuning, Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- 8 User-Selectable ÷ R Values — 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options — Single Ended (Three-State) or Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

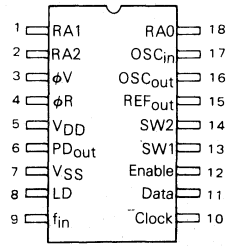


MC145155L1
CERAMIC PACKAGE
CASE 726

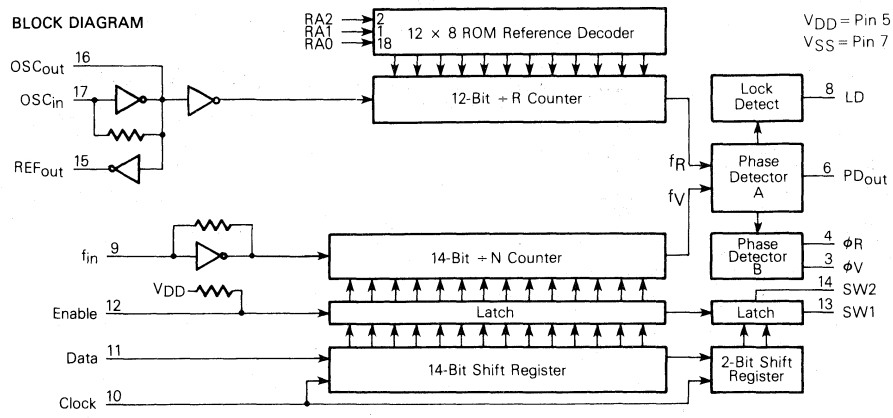


MC145155P1
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
V_{in}=0 V or V_{DD}		5	–	0.05	–	0.001	0.05	–	0.05	
I_{out}≈0 μA		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
V_{out}=0.5 V or V_{DD}−0.5 V		5	–	1.5	–	2.25	1.5	–	1.5	
(All Outputs Except OSC_{out})		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – SW1, SW2	I_{OL}									mA
V_{out}=0.3 V Sink		3	0.80	–	0.48	3.0	–	0.24	–	
V_{out}=0.4 V		5	1.50	–	0.90	3.6	–	0.45	–	
V_{out}=0.5 V		9	3.50	–	2.10	6.0	–	1.05	–	
Output Current – Other Outputs	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Data, Clock	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Current – Other Inputs	I_{IH}	9	–	0.3	–	0.00001	0.1	–	1.0	μA
(with Pullups)	I_{IL}	9	–	−400	–	−90	−200	–	−170	
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	μA
V_{in}=0 V or V_{DD}		5	–	1200	–	300	1200	–	2400	
I_{out}=0 μA		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current – PD_{out}	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA
V_{out}=0 V or 9 V										
Off-State Leakage Current – SW1, SW2 – V_{out}=9 V	I_{OZ}	9	–	0.3	–	0.0001	0.1	–	3.0	μA

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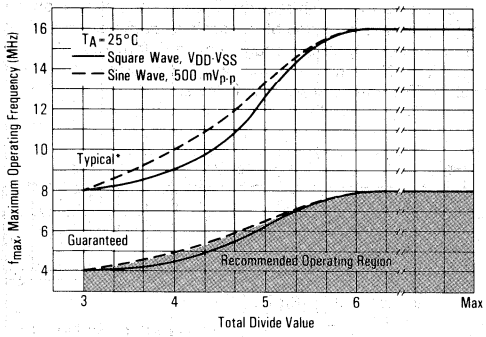
SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

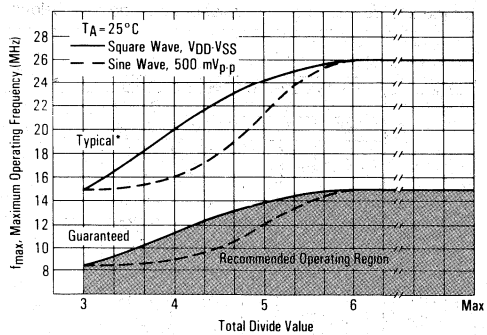
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time (Figures 1 and 7)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time	t_{PHL}	3	–	40	100	ns
Enable to SW1, SW2 (Figures 2 and 7)		5	–	25	40	
		9	–	15	25	
Setup Times	t_{su}	3	30	12	–	ns
Data to Clock (Figure 3)		5	20	10	–	
		9	18	9	–	
Clock to Enable (Figure 3)		3	70	30	–	
		5	32	16	–	
		9	25	12	–	
Hold Time	t_h	3	12	−8	–	ns
Clock to Data (Figure 3)		5	12	−6	–	
		9	15	−5	–	
Recovery Time	t_{rec}	3	5	−15	–	ns
Enable to Clock (Figure 3)		5	10	−8	–	
		9	20	0	–	
Output Pulse Width	$t_{w\phi}$	3	25	100	175	ns
ϕR, ϕV with f_R in Phase With f_V (Figures 4 and 7)		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times	t_r, t_f	3	–	20	5	μs
Any Input (Figure 5)		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width, Clock, Enable (Figure 6)	t_w	3	40	30	–	ns
		5	35	20	–	
		9	25	15	–	

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

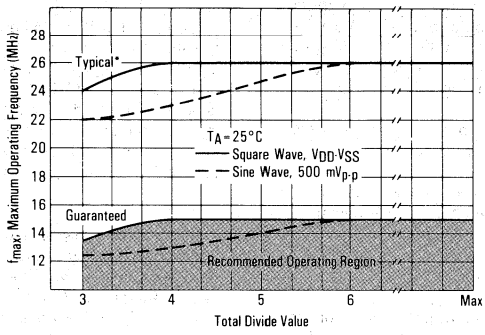
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

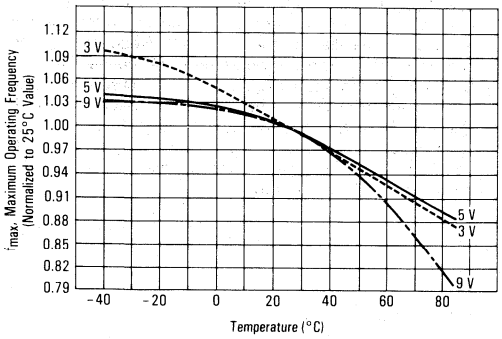


GRAPH 1C — V_{DD} = 9 V

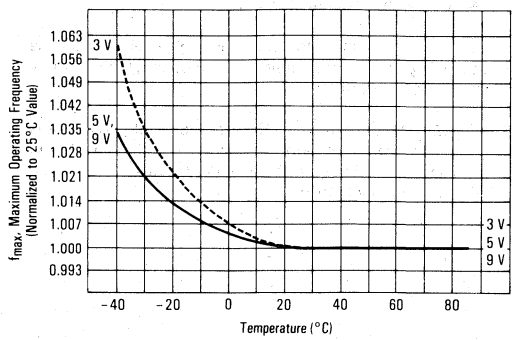


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



* Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

6

PIN DESCRIPTIONS

RA0, RA1, RA2 (Pins 18, 1, and 2) — These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

ϕV, ϕR (Pins 3 and 4) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

V_{DD} (Pin 5) — Positive power supply.

PD_{out} (Pin 6) — Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

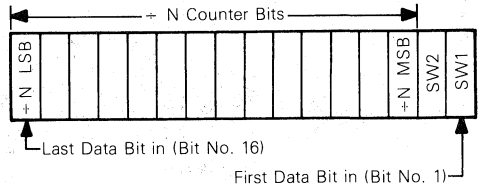
Frequency $f_V > f_R$ or f_V Leading: Negative Pulses.
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses.
Frequency $f_V = f_R$ and Phase Coincidence: High--Impedance State.

V_{SS} (Pin 7) — Circuit Ground.

LD (Pin 8) — Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

f_{in} (Pin 9) — Input to ÷ N portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 9. For larger amplitude signals (standard CMOS Logic levels) DC coupling may be used.

CLOCK, DATA (Pins 10 and 11) — Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 16-bit shift register. The data is presented on the DATA input at the time of the positive clock transition. The DATA input provides programming information for the 14-bit ÷ N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE (Pin 12) — When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pull-up establishes a continuously high level for ENABLE when no external signal is applied to Pin 12.

SW1, SW2 (Pins 13 and 14) — SW1 and SW2 provide latched open drain outputs corresponding to data bits numbers one and two. These will typically be used for band switch functions. A logic one will cause the output to assume a high-impedance state, while a logic zero will cause an output logic zero.

REF_{out} (Pin 15) — Buffered output of on-chip reference oscillator or externally provided reference-input signal.

OSC_{out}, OSC_{in} (Pins 16 and 17) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

SWITCHING WAVEFORMS

FIGURE 1

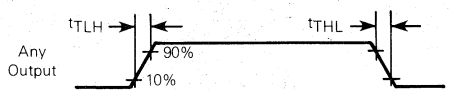


FIGURE 2

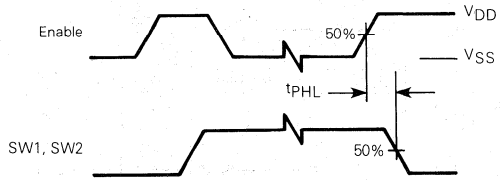


FIGURE 3

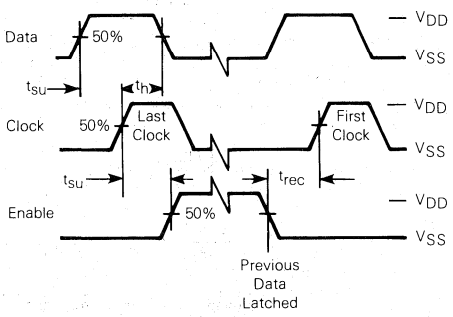
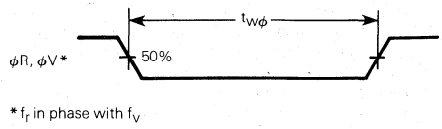


FIGURE 4



*f_r in phase with f_V

FIGURE 5

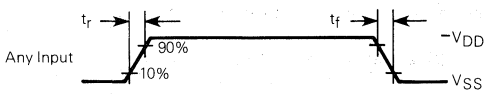


FIGURE 6

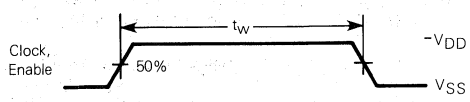
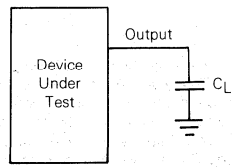


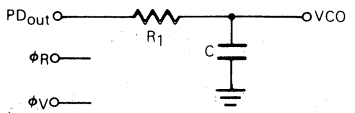
FIGURE 7 — TEST CIRCUIT



6

PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

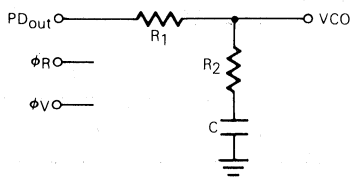


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

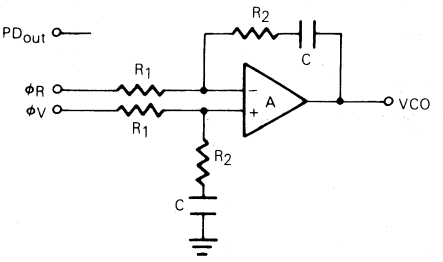


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

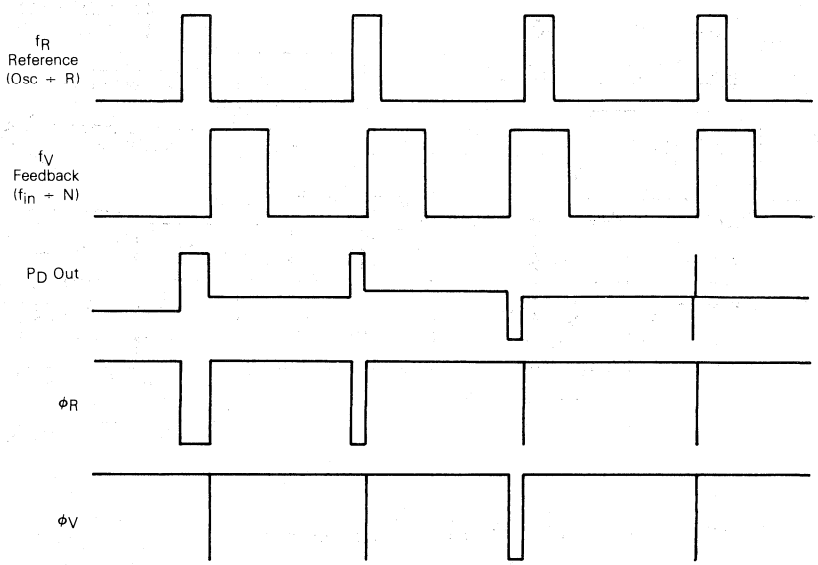
for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input),

$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

FIGURE 8
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

FIGURE 9 — TV/CATV TUNING SYSTEM

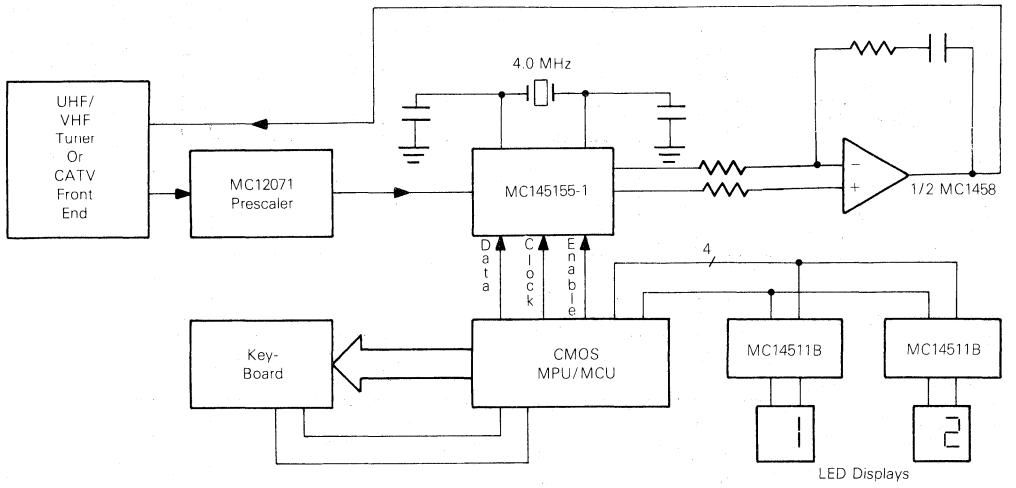
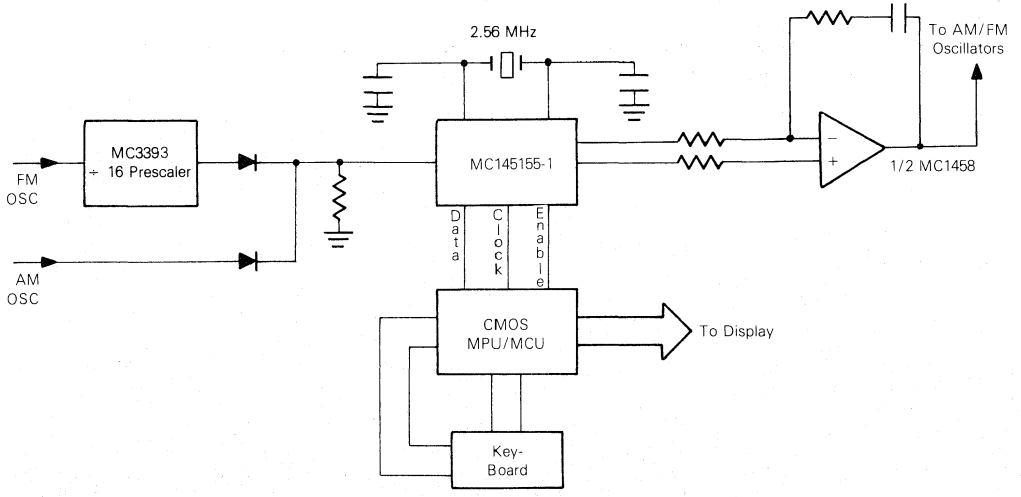


FIGURE 10 — FM/AM RADIO SYNTHESIZER



CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L=\frac{C_{in}C_{out}}{C_{in}+C_{out}}+C_a+C_O+\frac{C1\cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

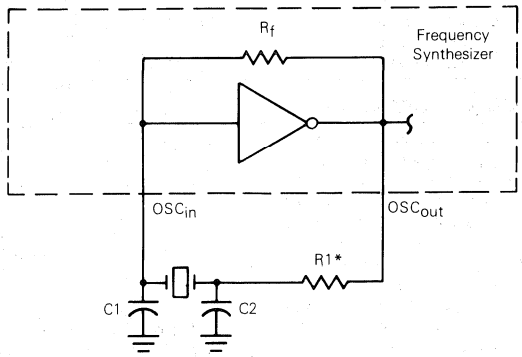
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

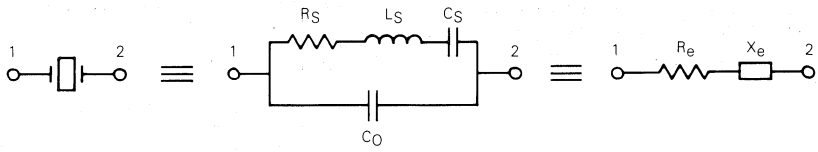
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



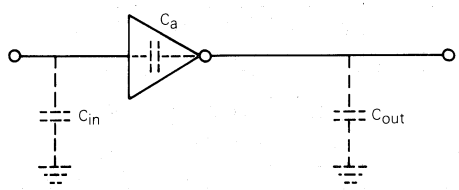
* May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES OF THE AMPLIFIER



MOTOROLA

MC145156-1

Advance Information

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

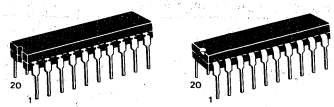
The MC145156-1 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable divide-by-A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156-1.

The MC145156-1 offers improved performance over the MC145156. Modulus Control output drive has been increased and the ac characteristics have been improved. Input current requirements have also been modified.

- General Purpose Applications:
  CATV, Two-Way Radios, Scanning Receivers, AM/FM Radios, TV Tuning, Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User-Selectable ÷ R Values — 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State)
  Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

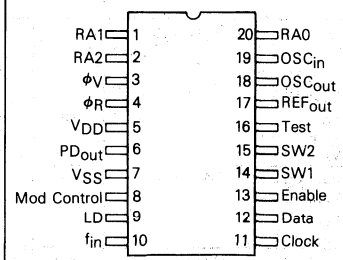
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

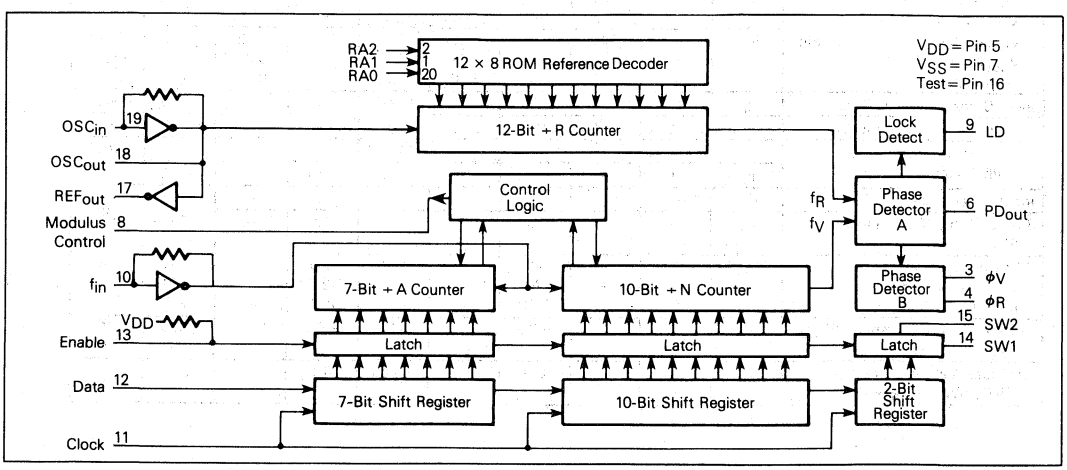


MC145156L1
CERAMIC PACKAGE
CASE 732

MC145156P1
PLASTIC PACKAGE
CASE 738

PIN ASSIGNMENT





This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

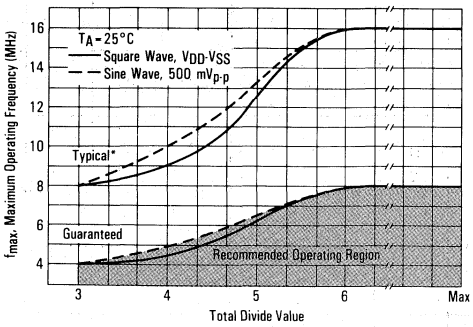
Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
V_{in} = 0 V or V_{DD}		5	–	0.05	–	0.001	0.05	–	0.05	
$I_{out} \approx 0$ μA		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
V_{out} = 0.5 V or V_{DD} − 0.5 V		5	–	1.5	–	2.25	1.5	–	1.5	
(All Outputs Except OSC_{out})		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – Modulus Control	I_{OH}									mA
V_{out} = 2.7 V Source		3	−0.60	–	−0.50	−1.5	–	−0.30	–	
V_{out} = 4.6 V		5	−0.90	–	−0.75	−2.0	–	−0.50	–	
V_{out} = 8.5 V		9	−1.50	–	−1.25	−3.2	–	−0.80	–	
V_{out} = 0.3 V Sink	I_{OL}	3	1.30	–	1.10	5.0	–	0.66	–	
V_{out} = 0.4 V		5	1.90	–	1.70	6.0	–	1.08	–	
V_{out} = 0.5 V		9	3.80	–	3.30	10.0	–	2.10	–	
Output Current – SW1, SW2	I_{OL}									mA
V_{out} = 0.3 V Sink		3	0.80	–	0.48	3.0	–	0.24	–	
V_{out} = 0.4 V		5	1.50	–	0.90	3.6	–	0.45	–	
V_{out} = 0.5 V		9	3.50	–	2.10	6.0	–	1.05	–	
Output Current – Other Outputs	I_{OH}									mA
V_{out} = 2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out} = 4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out} = 8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out} = 0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out} = 0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out} = 0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Data, Clock	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Current – Other Inputs	I_{IH}	9	–	0.3	–	0.00001	0.1	–	1.0	μA
(with Pullups)	I_{IL}	9	–	−400	–	−90	−200	–	−170	
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	μA
V_{in} = 0 V or V_{DD}		5	–	1200	–	300	1200	–	2400	
I_{out} = 0 μA		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current – PD_{out}	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA
V_{out} = 0 V or 9 V										
Off-State Leakage Current –	I_{OZ}	9	–	0.3	–	0.0001	0.1	–	3.0	μA
SW1, SW2 – V_{out} = 9 V										

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

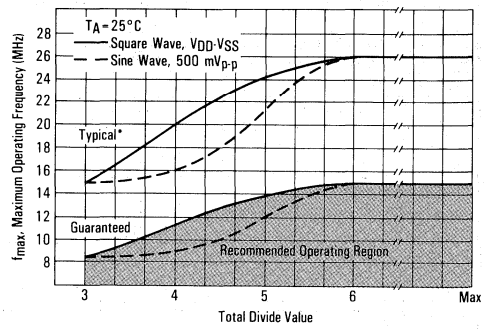
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 1 and 7)	t_{TLH}	3	–	50	115	ns
		5	–	30	60	
		9	–	20	40	
Output Fall Time, Modulus Control (Figures 1 and 7)	t_{THL}	3	–	25	60	ns
		5	–	17	34	
		9	–	15	30	
Output Rise and Fall Time, LD, ϕV, ϕR (Figures 1 and 7)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 2 and 7)	t_{PLH}, t_{PHL}	3	–	55	125	ns
		5	–	40	80	
		9	–	25	50	
Propagation Delay Time Enable to SW1, SW2 (Figures 2 and 7)	t_{PHL}	3	–	40	100	ns
		5	–	25	40	
		9	–	15	25	
Setup Times Data to Clock (Figure 3)	t_{su}	3	30	12	–	ns
		5	20	10	–	
		9	18	9	–	
Clock to Enable (Figure 3)		3	70	30	–	
		5	32	16	–	
		9	25	12	–	
Hold Time Clock to Data (Figure 3)	t_h	3	12	−8	–	ns
		5	12	−6	–	
		9	15	−5	–	
Recovery Time Enable to Clock (Figure 3)	t_{rec}	3	5	−15	–	ns
		5	10	−8	–	
		9	20	0	–	
Output Pulse Width ϕR, ϕV with f_R in Phase With f_V (Figures 4 and 7)	$t_{w\phi}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times Any Input (Figure 5)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width, Enable, Clock (Figure 6)	t_w	3	40	30	–	ns
		5	35	20	–	
		9	25	15	–	

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

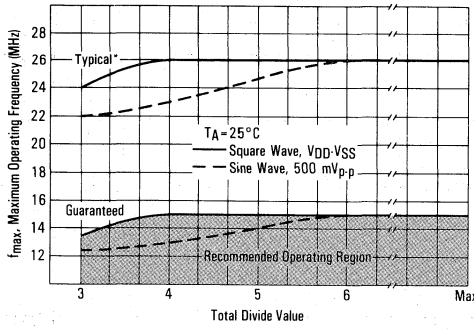
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

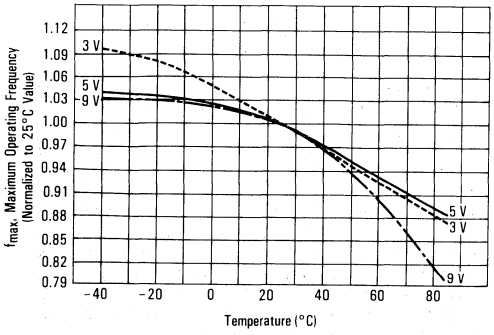


GRAPH 1C — V_{DD} = 9 V

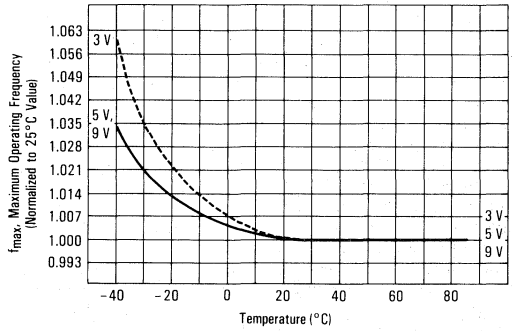


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

RA0, RA1, RA2 (Pins 20, 1, and 2) — These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

ϕV, ϕR (Pins 3 and 4) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of f_V = f_R and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

V_{DD} (Pin 5) — Positive power supply.

PD_{out} (Pin 6) — Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency f_V > f_R or f_V Leading: Negative Pulses
Frequency f_V < f_R or f_V Lagging: Positive Pulses
Frequency f_V = f_R and Phase Coincidence: High-Impedance State

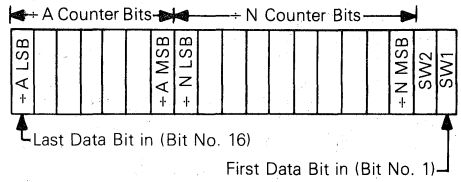
V_{SS} (Pin 7) — Circuit Ground.

MODULUS CONTROL (Pin 8) — Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N − A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for low and high modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the ÷A counter.

LD (Pin 9) — Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

f_{in} (Pin 10) — Input to the positive edge triggers ÷N and ÷A counters. f_{in} is typically derived from a dual modulus prescaler and is AC coupled into Pin 10. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

CLOCK, DATA (Pins 11 and 12) — Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 19-bit shift register. The data is presented on the DATA input at the time of the positive clock transition. The DATA input provides programming information for the 10-bit ÷N counter, the 7-bit ÷A counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE (Pin 13) — When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pull-up establishes a continuously high level for ENABLE when no external signal is applied to Pin 13.

SW1, SW2 (Pins 14 and 15) — SW1 and SW2 provide latched open drain outputs corresponding to data bits numbers one and two. These will typically be used for band switch functions. A logic one will cause the output to assume a high-impedance state, while a logic zero will cause an output logic zero.

TEST (Pin 16) — Used in manufacturing. Must be left open or tied to V_{SS}.

REF_{out} (Pin 17) — Buffered output of on-chip reference oscillator or externally provided reference-input signal.

OSC_{out}, OSC_{in} (Pins 18 and 19) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

6

SWITCHING WAVEFORMS

FIGURE 1

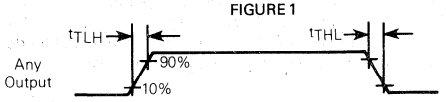


FIGURE 2

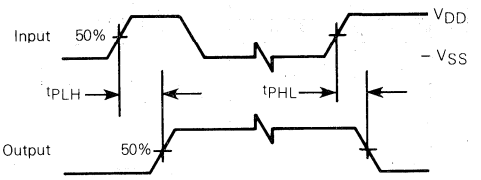


FIGURE 3

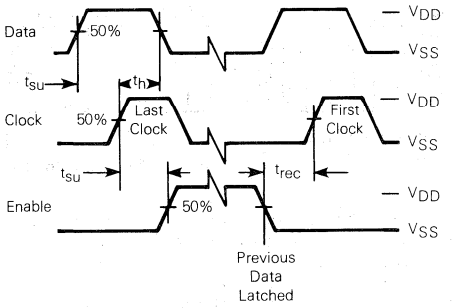
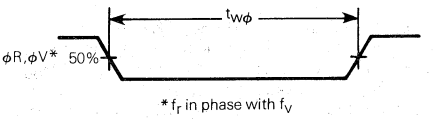


FIGURE 4



* f_r in phase with f_v

FIGURE 5

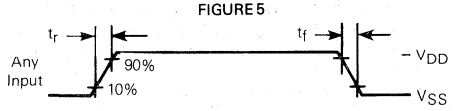


FIGURE 6

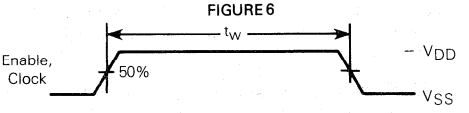
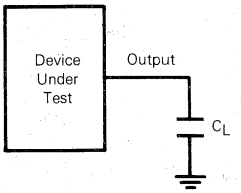
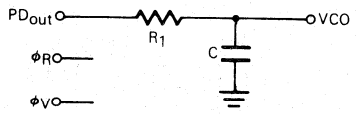


FIGURE 7 — TEST CIRCUIT



PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

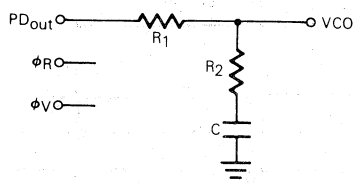


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

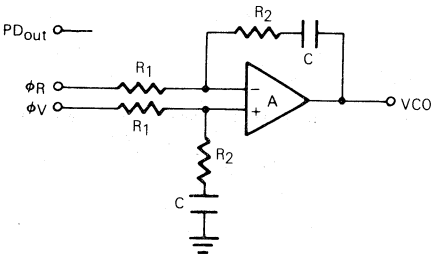


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_n \cong \frac{2\pi fr}{10}$ (at phase detector input),

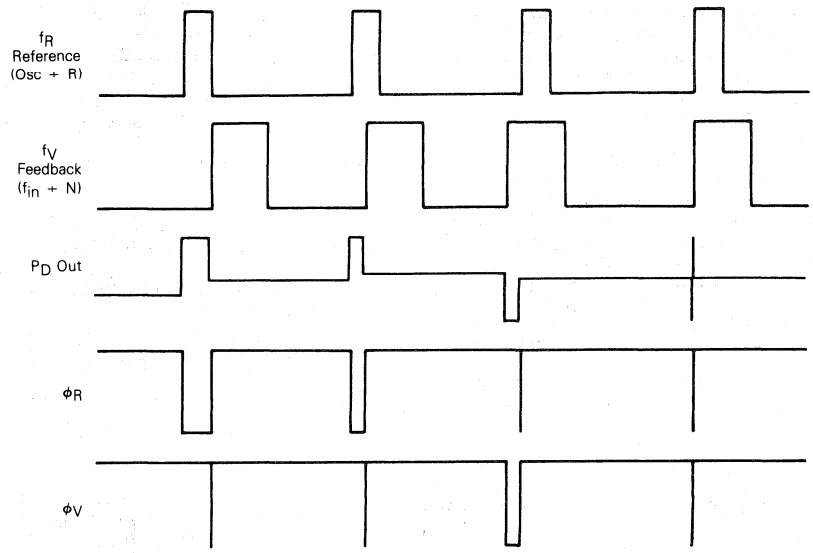
$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

FIGURE 8

PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

DUAL MODULUS PRESCALING

For the following text, the dash number has been omitted from the part number for simplicity.

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145156 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by the MC145156.

Several dual modulus prescaler approaches suitable for use with the MC145156 are given in Figure 9. The approaches range from the low cost ÷15/÷16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145156 and dual modulus prescaling are shown in Figures 10 and 11 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145156

The system total divide value (N_{total}) will be dictated by the application. i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷N counter; A is the number programmed into the ÷A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P − 1 for a particular value N in the divide N counter. N is then incremented to N + 1 and the ÷A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the ÷N and ÷A counters. The constraint N ≥ A always applies. If $A_{max} = P - 1$ then $N_{min} \geq P - 1$. Then $N_{total-min} = (P-1)P + A$ or $(P-1)P$ since A is free to assume the value of zero.

$$N_{total-max} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of Pin 10 of the MC145156.

B. The period of f_{VCO}, divided by P, must be greater than the sum of the times:
   a. Propagation delay through the dual modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the MC145156.

A sometimes useful simplification in the MC145156 programming code can be achieved by choosing the values for P of 8, 16, 32, 64 or 128. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

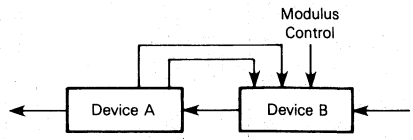
A. Assume the ÷A counter contains "b" bits where $2^b = P$.
B. Always program all higher order ÷A counter bits above "b" to zero.
C. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10 + b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10 + b bit counter.

FIGURE 9 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145156

MC12009	÷5/÷6	440 MHz Min
MC12011	÷8/÷9	500 MHz Min
MC12013	÷10/÷11	500 MHz Min
MC12015	÷32/÷33	225 MHz Min
MC12016	÷40/÷41	225 MHz Min
MC12017	÷64/÷65	225 MHz Min
*MC12018	÷128/÷129	520 MHz Min
MC3393	÷15/÷16	140 MHz Typ

*Proposed introduction

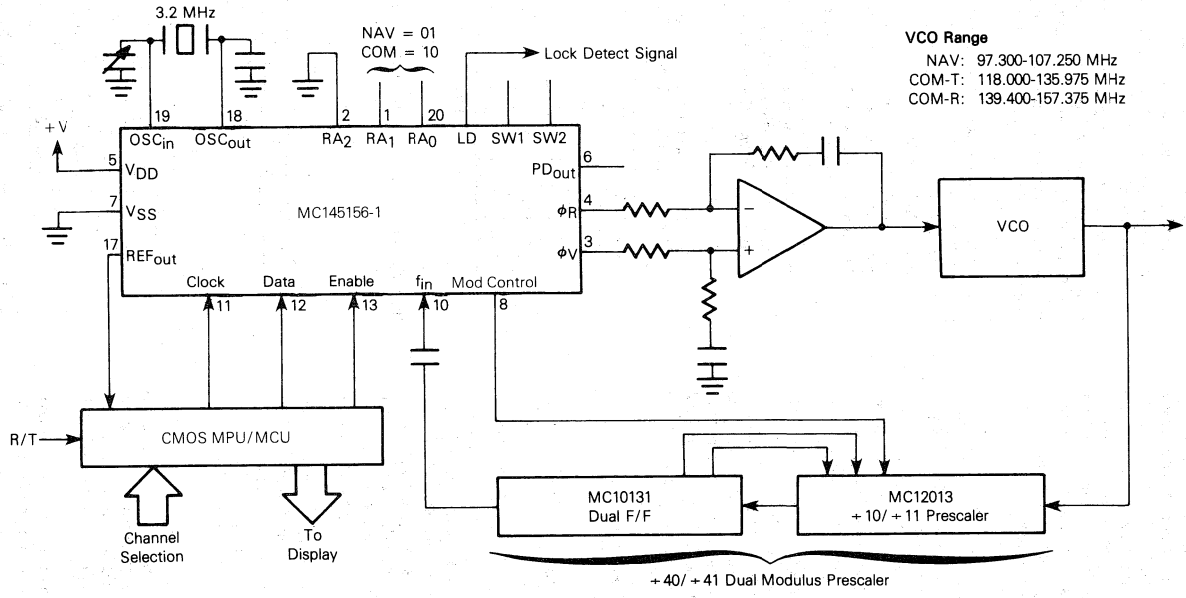
By using two devices several dual modulus values are achievable:



Device A \ Device B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 or ÷80/÷81	÷64/÷65 or ÷128/÷129	÷80/÷81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent
MC12015, MC12016, and MC12017 are pin equivalent.

FIGURE 10 — AVIONICS NAV AND COM SYNTHESIZER



NOTES:
1) for NAV: $F_R = 50$ kHz, ÷R = 64 using 10.7 MHz lowside injection, $N_{total} = 1946\text{-}2145$
   for COM-T $F_R = 25$ kHz, ÷R = 128 using 21.4 MHz highside injection, $N_{total} = 4720\text{-}5439$
   for COM-R $F_R = 25$ kHz, ÷R = 128 using 21.4 MHz highside injection, $N_{total} = 5576\text{-}6295$
2) A ÷32/÷33 dual modulus approach is provided by substituting an MC12011 (÷8/÷9) for the MC12013. The devices are pin equivalent.
3) A 6.4 MHz oscillator crystal can be used by selecting ÷R = 128 (code 010) for NAV and ÷R = 256 (code 011) for COM

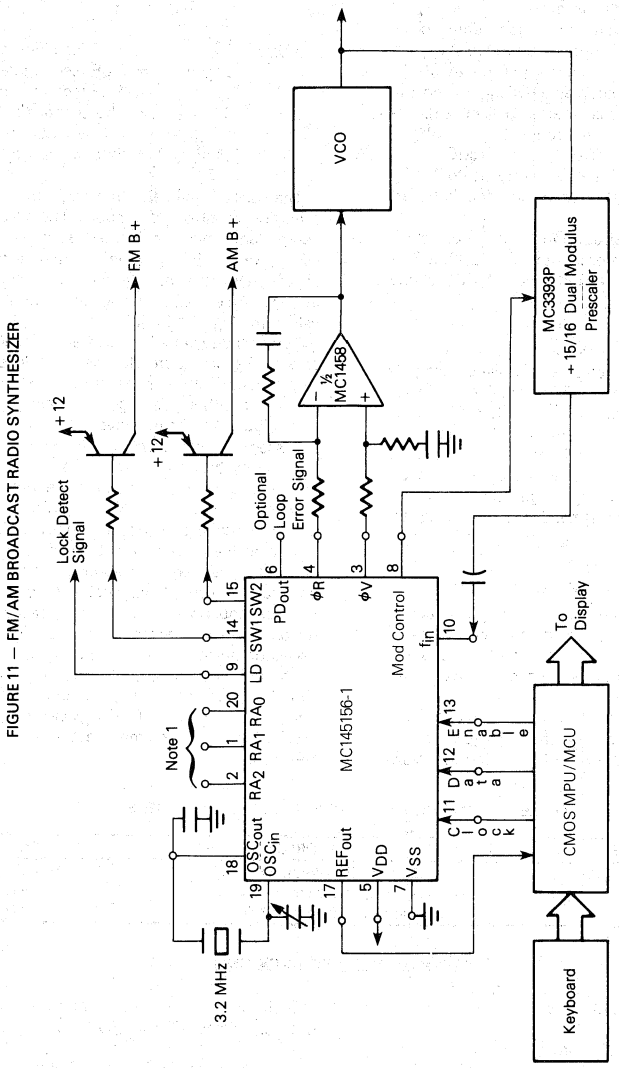


FIGURE 11 — FM/AM BROADCAST RADIO SYNTHESIZER

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

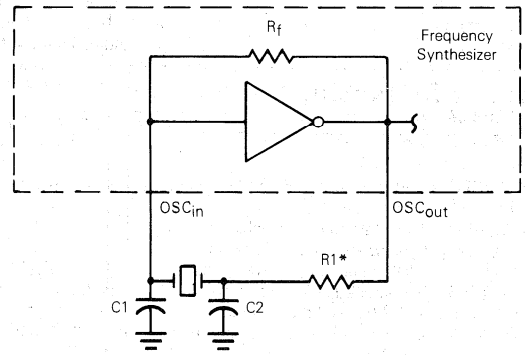
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

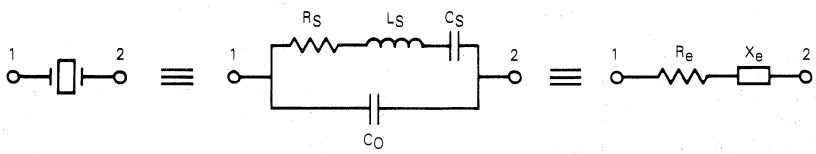
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



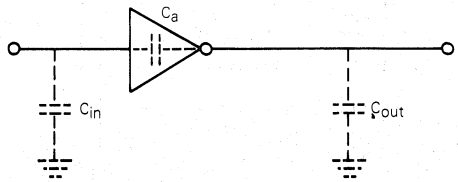
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES
OF THE AMPLIFIER



MOTOROLA

MC145157-1
MC145158-1

Advance Information

SERIAL INPUT PLL FREQUENCY SYNTHESIZERS

The MC145157-1 and MC145158-1 have fully programmable 14-bit reference counters, as well as fully programmable ÷ N (MC145157-1) and ÷ N/ ÷ A (MC145158-1) counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

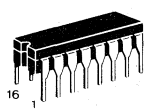
When combined with a loop filter and VCO, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed-divide prescaler can be used between the VCO and the PLL for the MC145157-1 and a dual-modulus prescaler for the MC145158-1.

The MC145157-1 and MC145158-1 offer improved performance over the MC145157 and MC145158. Modulus Control output drive has been increased and the ac characteristics have been improved. Input current requirements have also been modified.

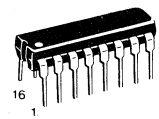
- General Purpose Applications:
  CATV
  AM/FM Radios
  Two-Way Radios
  TV Tuning
  Scanning Receivers
  Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383 for the MC145157-1
  − 3 to 1023 for the MC145158-1
- Dual Modulus Capability for the MC145158-1
  ÷ A Range = 0 to 127
- f_V and f_r Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

SERIAL INPUT PLL FREQUENCY SYNTHESIZER



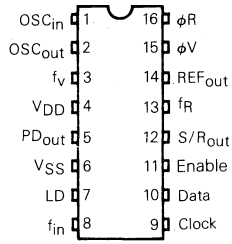
MC145157L1
MC145158L1
CERAMIC PACKAGE
CASE 620



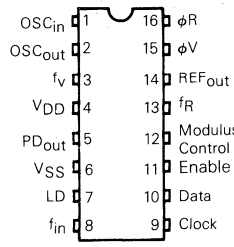
MC145157P1
MC145158P1
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT

MC145157-1



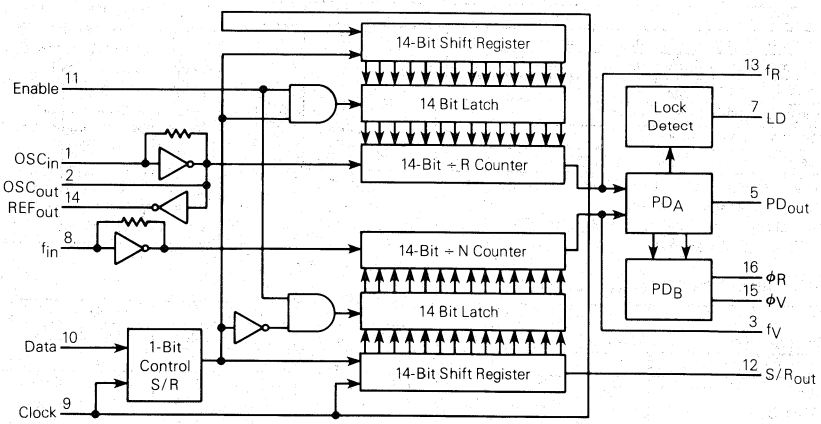
MC145158-1



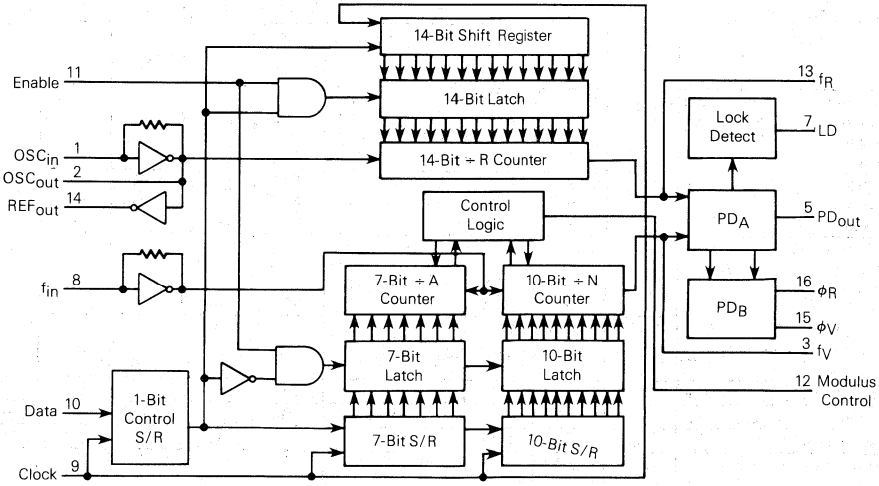
6

This is advance information and specifications are subject to change without notice.

MC145157-1



MC145158-1



V_{DD} = Pin 4
V_{SS} = Pin 6

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

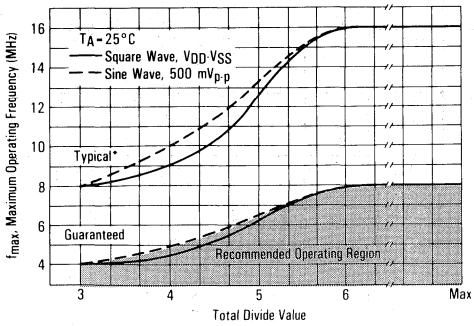
Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
V_{in} = 0 V or V_{DD}		5	–	0.05	–	0.001	0.05	–	0.05	
$I_{out} \approx 0$ μA		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
V_{out} = 0.5 V or V_{DD} − 0.5 V		5	–	1.5	–	2.25	1.5	–	1.5	
(All Outputs Except OSC_{out})		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – Modulus Control	I_{OH}									mA
V_{out} = 2.7 V Source		3	−0.60	–	−0.50	−1.5	–	−0.30	–	
V_{out} = 4.6 V		5	−0.90	–	−0.75	−2.0	–	−0.50	–	
V_{out} = 8.5 V		9	−1.50	–	−1.25	−3.2	–	−0.80	–	
V_{out} = 0.3 V Sink	I_{OL}	3	1.30	–	1.10	5.0	–	0.66	–	
V_{out} = 0.4 V		5	1.90	–	1.70	6.0	–	1.08	–	
V_{out} = 0.5 V		9	3.80	–	3.30	10.0	–	2.10	–	
Output Current – Other Outputs	I_{OH}									mA
V_{out} = 2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out} = 4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out} = 8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out} = 0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out} = 0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out} = 0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Data, Clock, Enable	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current	I_{DD}	3	–	800	–	200	800	–	1600	μA
V_{in} = 0 V or V_{DD}		5	–	1200	–	300	1200	–	2400	
I_{out} = 0 μA		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current – PD_{out}	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA
V_{out} = 0 V or 9 V										

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

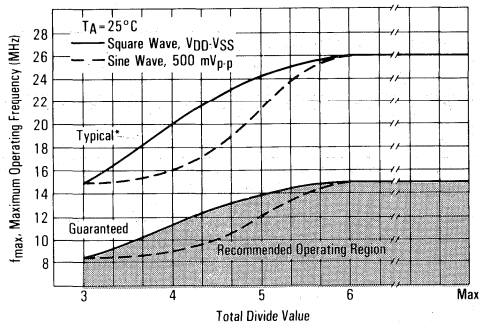
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 2 and 8)	t_{TLH}	3	–	50	115	ns
		5	–	30	60	
		9	–	20	40	
Output Fall Time, Modulus Control (Figures 2 and 8)	t_{THL}	3	–	25	60	ns
		5	–	17	34	
		9	–	15	30	
Output Rise and Fall Time, LD, f_V, f_R, S/R_{out}, ϕV, ϕR (Figures 2 and 8)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 3 and 8)	t_{PLH}, t_{PHL}	3	–	55	125	ns
		5	–	40	80	
		9	–	25	50	
Setup Times	t_{su}					ns
Data to Clock (Figure 4)		3	30	12	–	
		5	20	10	–	
		9	18	9	–	
Clock to Enable (Figure 4)		3	70	30	–	
		5	32	16	–	
		9	25	12	–	
Hold Time Clock to Data (Figure 4)	t_h	3	12	−8	–	ns
		5	12	−6	–	
		9	15	−5	–	
Recovery Time Enable to Clock (Figure 4)	t_{rec}	3	5	−15	–	ns
		5	10	−8	–	
		9	20	0	–	
Output Pulse Width ϕR, ϕV with f_R in Phase with f_V (Figures 5 and 8)	$t_{w\phi}$	3	25	100	175	ns
		5	20	60	100	
		9	10	40	70	
Input Rise and Fall Times Any Input (Figure 6)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width, Enable, Clock (Figure 7)	t_w	3	40	30	–	ns
		5	35	20	–	
		9	25	15	–	

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

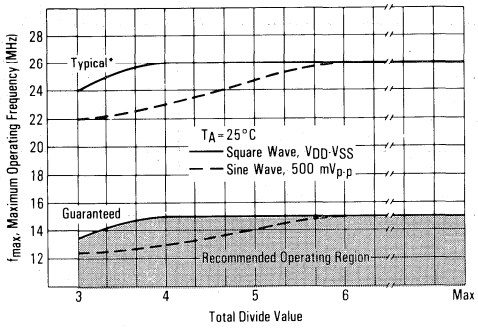
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

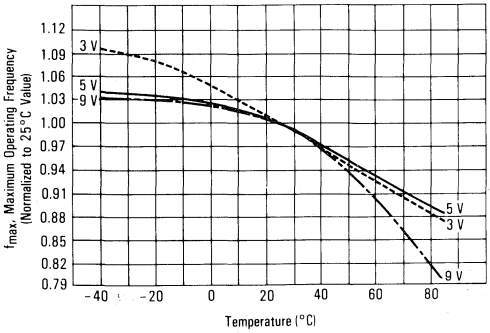


GRAPH 1C — V_{DD} = 9 V

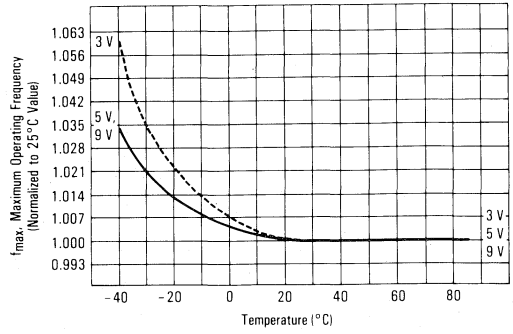


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

For the following text, the dash number has been omitted from the part number for simplicity.

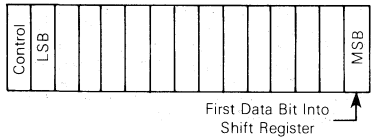
INPUTS

OSC_{in}, OSC_{out} (Pins 1, 2) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

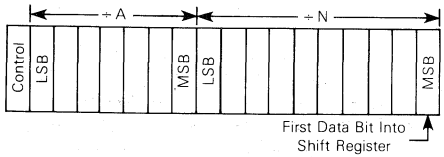
f_{in} (Pin 8) — Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter (÷ A or ÷ N counter for the MC145158). This input has an inverter biased in the linear region to allow use with AC signals as low as 500 mV p-p or with a square wave of V_{DD} to V_{SS}.

Clock, Data (Pins 9, 10) — Shift register clock and data input. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the ÷ N counter latch (÷ A, ÷ N counter latch for the MC145158). The data entry format is as follows:

MC145157 ÷ R and ÷ N Data Input
MC145158 ÷ R Data Input



MC145158 ÷ A, ÷ N Data Input



OUTPUTS

f_R, f_V (Pins 13, 3) — Divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

PD_{out} (Pin 5) — Single ended (three-state) phase detector output. This output produces a loop error signal that is used with a loop filter to control a VCO. This phase detector output is described below and illustrated in Figure 9.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕ_R, ϕ_V (Pins 16, 15) — Double-ended phase detector outputs. These outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high (see Figure 9 for illustration).

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low; ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

S/R_{out} (Pin 12 of the MC145157) — Shift register output. This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

Modulus Control (Pin 12 of the MC145158) — Modulus control output. This output generates a signal by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N — A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual modulus version offers a distinct advantage. The dual modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

LD (Pin 7) — Lock detect signal. This output is at a high logic level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when the loop is out of lock.

REF_{out} (Pin 14) — Buffered reference oscillator output. This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

CONTROLS

Enable (Pin 11) — Latch Enable Input. A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency

6

synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145158 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by the MC145158.

Several dual modulus prescaler approaches suitable for use with the MC145158 are given in Figure 1. The approaches range from the low cost ÷15/÷16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz.

DESIGN GUIDELINES APPLICABLE TO THE MC145158

The system total divide value (N_{total}) will be dictated by the application, i.e.

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷N counter; A is the number programmed into the ÷A counter. P and P + 1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P − 1 for a particular value N in the ÷N counter. N is then incremented to N + 1 and the ÷A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the ÷N and ÷A counters. the constraint $N \geq A$ always applies. If $A_{max} = P - 1$ the $N_{min} \geq P - 1$. Then $N_{(total-min)} = (P-1)P + A$ or $(P-1)P$ since A is free to assume the value of zero.

$$N_{(total-max)} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler ($F_{VCO}max$), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of Pin 8 of the MC145158.

B. The period of $f_{VCO(max)}$, divided by P, must be greater than the sum of the times:

   a. Propagation delay through the dual modulus prescaler.

   b. Prescaler setup or release time relative to its modulus control signal.

   c. Propagation time from f_{in} to the modulus control output for the MC145158.

A sometimes useful simplification in the MC145158 programming code can be achieved by choosing the values for P of 8, 16, 32, 64 or 128. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

A. Assume the ÷A counter contains "b" bits where $2^b = P$.

B. Always program all higher order ÷A counter bits above "b" to zero.

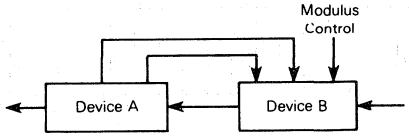
C. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10 + b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10 + b bit counter.

FIGURE 1 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145158

MC12009	÷5/÷6	440 MHz Min
MC12011	÷8/÷9	500 MHz Min
MC12013	÷10/÷11	500 MHz Min
MC12015	÷32/÷33	225 MHz Min
MC12016	÷40/÷41	225 MHz Min
MC12017	÷64/÷65	225 MHz Min
*MC12018	÷128/÷129	520 MHz Min
MC3393	÷15/÷16	140 MHz Typ

*Proposed Introduction 1983

By using two devices several dual modulus values are achievable:



Device A \ Device B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 or ÷80/÷81	÷64/÷65 or ÷128/÷129	÷80/÷81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

SWITCHING WAVEFORMS

FIGURE 2

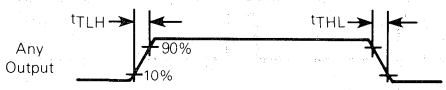


FIGURE 3

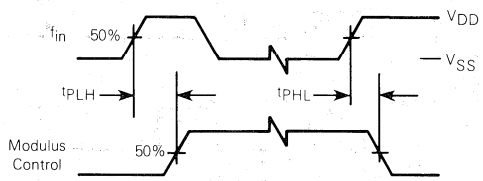


FIGURE 4

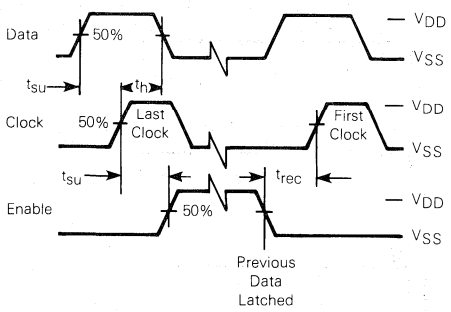


FIGURE 5

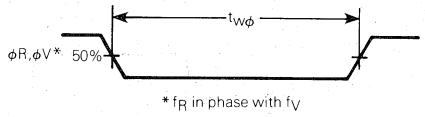


FIGURE 6

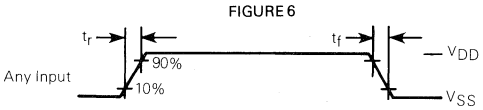


FIGURE 7

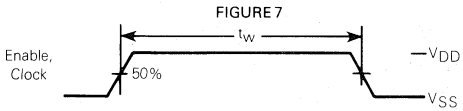


FIGURE 8 — TEST CIRCUIT

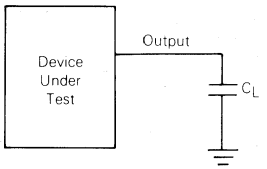


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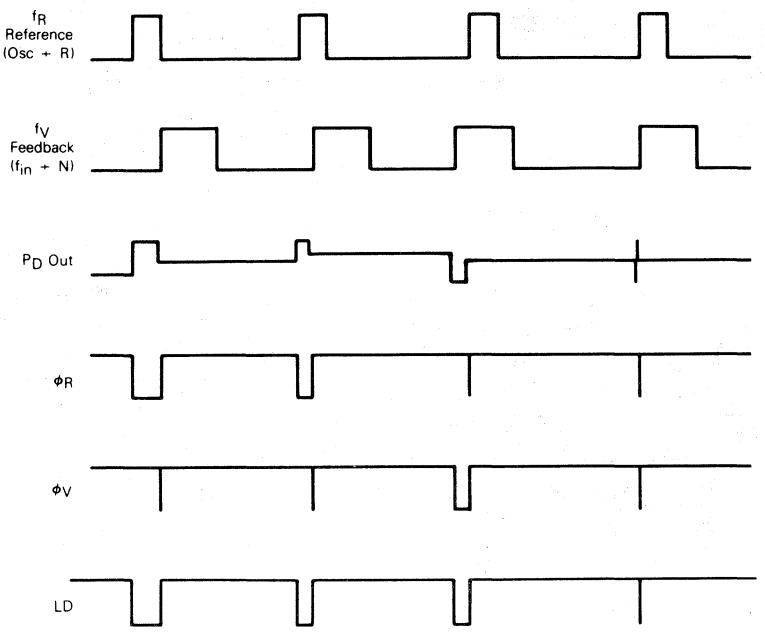
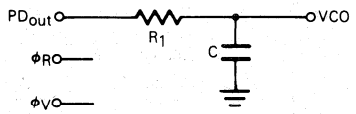
FIGURE 9
PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is approximately equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

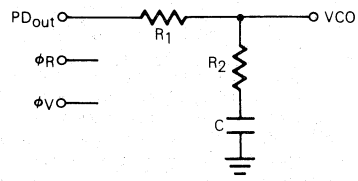


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

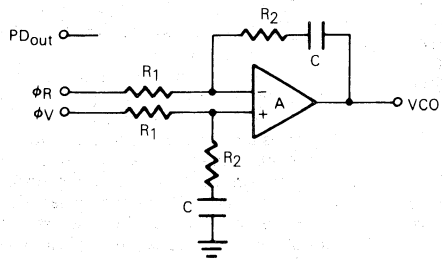


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input),

$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

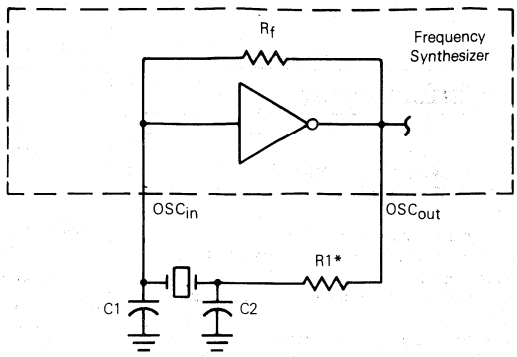
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

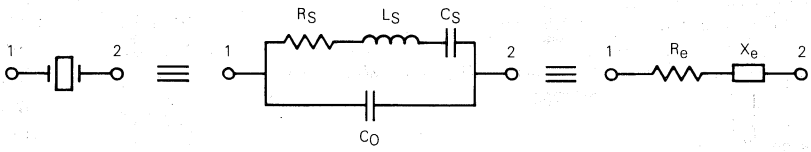
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



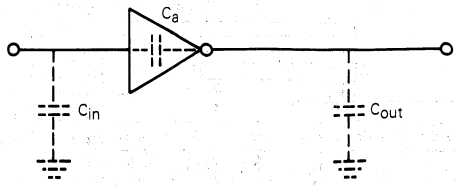
*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES OF THE AMPLIFIER



6

MOTOROLA

MC145159-1

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

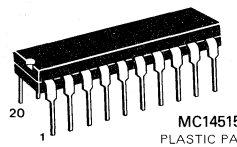
SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH ANALOG PHASE DETECTOR

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH ANALOG PHASE DETECTOR

The MC145159-1 has a programmable 14-bit reference counter, as well as programmable divide-by-N/divide-by-A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

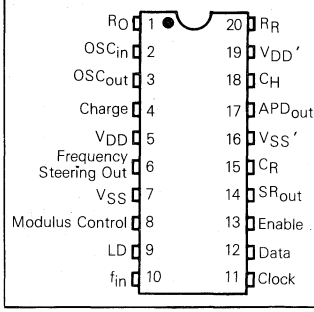
When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual modulus prescaler can be used between the VCO and the PLL.

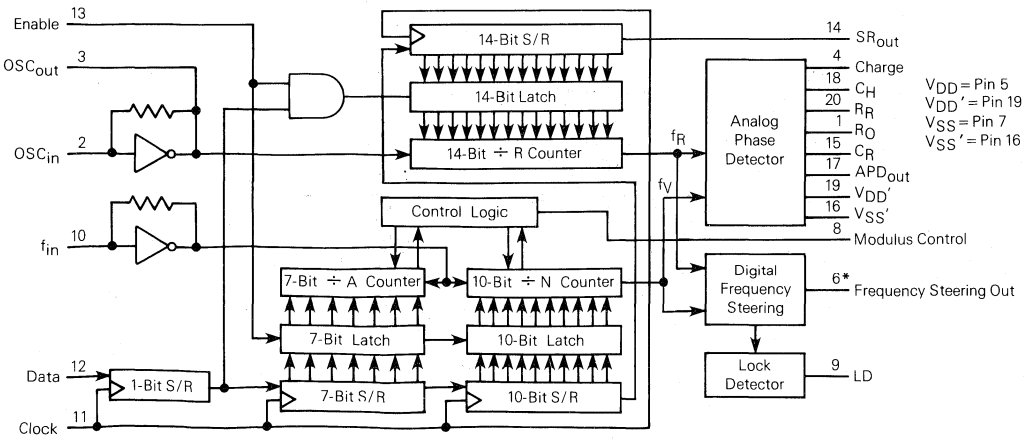
- General Purpose Applications:
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two Way Radios — Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Dual Modulus
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, ÷ A Range = 0 to 127
- High-Gain Analog Phase Detector



MC145159P1
PLASTIC PACKAGE
CASE 738

PIN ASSIGNMENT





*Note: Pin 6 is not and cannot be used as a digital phase detector output.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level V_{in}=0 V or V_{DD} I_{out}≈0 μA	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
		5	–	0.05	–	0.001	0.05	–	0.05	
		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95		
		9	8.95	–	8.95	8.999	–	8.95	–	
△Voltage, $V_{CH}-V_{APD_{out}}$ $I_{APD_{out}}$≈0 μA	△V	–					1.05			V
Input Voltage 0 Level V_{out}=0.5 V or V_{DD}−0.5 V (All Outputs Except OSC_{out})	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
		5	–	1.5	–	2.25	1.5	–	1.5	
		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current – Modulus Control	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.60	–	−0.50	−1.5	–	−0.30	–	
V_{out}=4.6 V		5	−0.90	–	−0.75	−2.0	–	−0.50	–	
V_{out}=8.5 V		9	−1.50	–	−1.25	−3.2	–	−0.80	–	
V_{out}=0.3 V Sink	I_{OL}	3	1.30	–	1.10	5.0	–	0.66	–	
V_{out}=0.4 V		5	1.90	–	1.70	6.0	–	1.08	–	
V_{out}=0.5 V		9	3.80	–	3.30	10.0	–	2.10	–	
Output Current, C_R V_{CR}=4.5 V, R_R=240 k	I_{CR}	9			−100		−120			μA
Output Current, APD_{out} R_o=240 k, V_{CH}=0 V $V_{APD_{out}}$=4.5 V	I_{APD}	9			170		350			μA
Output Current – Other Outputs	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current – Data, Clock, Enable	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current – f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance – Frequency Steering Out	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 μA	I_{DD}	3	–	800	–	200	800	–	1600	μA
		5	–	1200	–	300	1200	–	2400	
		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current V_{out}=0 V or 9 V	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA

6

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise Time, Modulus Control (Figures 3 and 8)	t_{TLH}	3	–	50	115	ns
		5	–	30	60	
		9	–	20	40	
Output Fall Time, Modulus Control (Figures 3 and 8)	t_{THL}	3	–	25	60	ns
		5	–	17	34	
		9	–	15	30	
Output Rise and Fall Time, LD (Figures 3 and 8)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Propagation Delay Time f_{in} to Modulus Control (Figures 4 and 8)	t_{PLH}, t_{PHL}	3	–	55	125	ns
		5	–	40	80	
		9	–	25	50	
Setup Times	t_{su}					ns
Data to Clock (Figure 5)		3	30	12	–	
		5	20	10	–	
		9	18	9	–	
Clock to Enable (Figure 5)		3	70	30	–	
		5	32	16	–	
		9	25	12	–	
Hold Time Clock to Data (Figure 5)	t_h	3	12	−8	–	ns
		5	12	−6	–	
		9	15	−5	–	
Recovery Time Enable to Clock (Figure 5)	t_{rec}	3	5	−15	–	ns
		5	10	−8	–	
		9	20	0	–	
Input Rise and Fall Times Clock, OSC_{in}, f_{in} (Figure 6)	t_r, t_f	3	–	20	5	μs
		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width, Enable, Clock (Figure 7)	t_w	3	40	30	–	ns
		5	35	20	–	
		9	25	15	–	

PIN DESCRIPTIONS

INPUTS

OSC_{in}, OSCILLATOR INPUT (PIN 2), OSC_{out}, OSCILLATOR OUTPUT (PIN 3) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of an appropriate value must be connected from OSC_{in} to V_{SS} and OSC_{out} to V_{SS}. OSC_{in} may also serve as input for an externally generated reference signal. This signal will typically be ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

f_{in}, FREQUENCY IN (PIN 10) — Input to the positive edge triggered divide-by-N and divide-by-A counters. f_{in} is typically derived from a dual modulus prescaler and is ac coupled into Pin 10. This input has an inverter biased in the linear region to allow use with ac-coupled signals as low as 500 mV peak-to-peak or direct-coupled signals swinging from V_{DD} to V_{SS}.

Data, SERIAL DATA INPUT (PIN 12) — Counter and control information is shifted into this input. The last data bit entered goes into the one-bit control shift register. A logic one allows the reference counter information to be loaded into it's 14-bit latch when Enable goes high. A logic zero entered as the control bit disables the reference counter latch. The divide-by-A/divide-by-N counter latch is loaded, regardless of the contents of the control register, when Enable goes high. The data entry format is shown below.

Enable, TRANSPARENT LATCH ENABLE (PIN 13) — A high on this input allows data to be entered into the divide-by-A/divide-by-N latch and, if the control bit is high, into the reference counter latch. Counter programming is unaffected when Enable is low.

Clock, SHIFT REGISTER CLOCK (PIN 11) — A low-to-high transition on this input shifts data from the Serial Data input into the shift registers.

COMPONENT PINS

C_R, RAMP CAPACITOR (PIN 15) — The capacitor connected from this pin to V_{SS} is charged linearly, at a rate determined by R_R. The voltage on this capacitor is proportional to the phase difference of the frequencies present at the internal phase detector inputs. A polystyrene or mylar capacitor is recommended.

R_R, RAMP CURRENT BIAS RESISTOR (PIN 20) — A resistor connected from this pin to V_{SS} determines the rate at which the ramp capacitor is charged, thereby affecting the phase detector gain (see Figure 1).

C_H, HOLD CAPACITOR (PIN 18) — The charge stored on the ramp capacitor is transferred to the capacitor connected from this pin to either V_{DD}' or V_{SS}'. The ratio of C_R to C_H should be large enough to have no affect on the phase detector gain ($C_R > 10C_H$). A low-leakage capacitor should be used.

R_O, OUTPUT BIAS CURRENT RESISTOR (PIN 1) — A resistor connected from this pin to V_{SS} biases the output N-Channel transistor, thereby setting a current sink on the Analog Phase Detector Output (Pin 17). This resistor adjusts the VCO input voltage change with respect to phase error (see Figure 2).

OUTPUTS

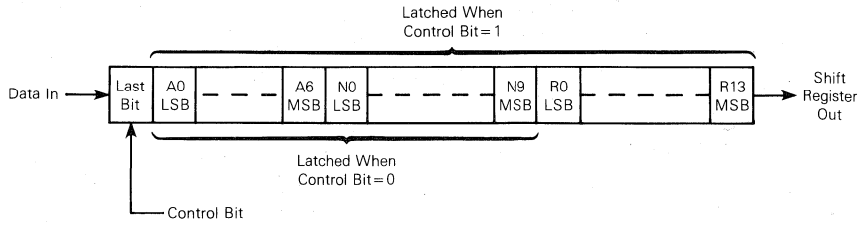
APD_{out}, ANALOG PHASE DETECTOR OUTPUT (PIN 17) — This output produces a voltage that controls an external VCO. The voltage range of this output ($V_{DD} = +9$ V) is from below $+0.5$ V to $+8$ V or more. The source impedance of this output is the equivalent of a source follower with an externally variable source resistor. The source resistor depends upon the output bias current controlled by the output bias current resistor, R_O. The bias current is adjustable from 0.01 mA to 0.5 mA. The output voltage will not be more than 1.05 V below the sampled point on the ramp. With a constant sample of the ramp voltage at 9 V and the hold capacitor at 50 pF, the instantaneous output ripple is not greater than 5 mV peak-to-peak.

Charge, RAMP CHARGE INDICATOR (PIN 4) — This output is high from the time f_R goes high to the time f_V goes high (f_R and f_V are the frequencies at the phase detector inputs). This high voltage indicates that the ramp capacitor, C_R, is being charged.

Frequency Steering Out, THREE-STATE FREQUENCY STEERING OUTPUT (PIN 6) — If the counted down input frequency on f_{in} is higher than the counted down reference frequency of OSC_{in}, this output goes low. If the counted down VCO frequency is lower than that of the counted down OSC_{in}, this output goes high.

The repetition rate of the Frequency Steering Output pulses is approximately equal to the difference of the frequencies of the two counted down inputs from the VCO and

DATA ENTRY FORMAT



OSC_{in}. The output maintains a high-impedance state when the counted down VCO (divided down f_{in} pulse) and the counted down OSC_{in} are in a one-to-one ratio over a 2π window with respect to the counted down OSC_{in}.

LD, PHASE LOCK INDICATOR (PIN 9) — This output is high during lock and goes low to indicate a non-lock condition. The frequency and duration of the non-lock pulses will be the same as either polarity of the Frequency Steering Output.

Modulus Control, DUAL MODULUS PRESCALER CONTROL (PIN 8) — The modulus control level is low at the beginning of a count cycle and remains low until the divide-by-A counter has counted down from its programmed value. At that time, the modulus control goes high and remains high until the divide-by-N counter has counted the rest of the way down from its programmed value (N − A additional counts, since both divide-by-N and divide-by-A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence is repeated. This provides a total programmable divide value of $N_T = N \cdot P + A$, where P and P+1 represent the dual modulus prescaler divide values, respectively, for high and low Modulus Control levels; N is the number programmed into the divide-by-N counter, and A is the number programmed into the divide-by-A counter.

SR_{out}, SHIFT REGISTER OUTPUT (PIN 14) — This pin is the non-inverted output of the inner-most bit of the 32-bit Serial Data Shift Register. It is not latched by the Enable line.

POWER PINS

V_{DD}, POSITIVE POWER SUPPLY (PIN 5) — Positive power supply input for all sections of the MC145159-1 except the Analog Phase Detector. V_{DD} and V_{DD}' should be powered up at the same time to avoid damage to the MC145159-1.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 7) — Circuit ground for all sections of the MC145159-1 except the Analog Phase Detector.

V_{SS}', ANALOG PHASE DETECTOR CIRCUIT GROUND (PIN 16), V_{DD}', ANALOG POWER SUPPLY (PIN 19) — Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

FIGURE 1 — CHARGE CURRENT vs RAMP RESISTANCE

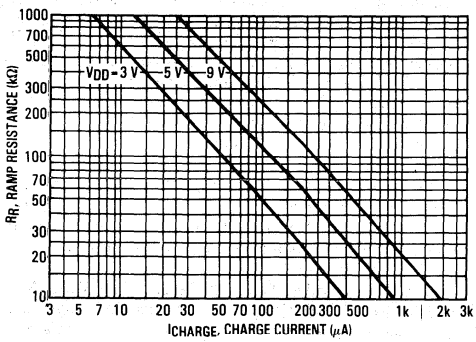
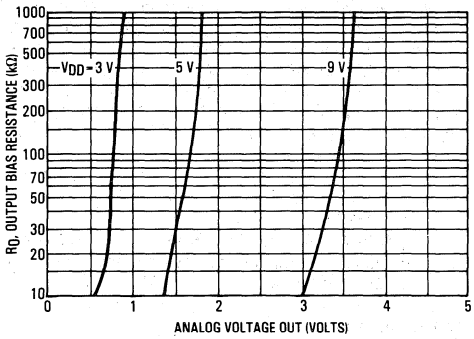


FIGURE 2 — VCO BIAS VOLTAGE



DESIGN EQUATION

$$K_\phi = \frac{I_{charge}}{2\pi f_R C_R}$$

where K_ϕ = phase detector gain, I_{charge} is from Figure 1
f_R = reference frequency, C_R = ramp capacitor (in farads)

SWITCHING WAVEFORMS

FIGURE 3

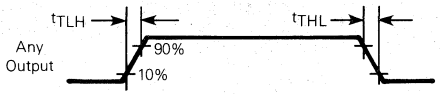


FIGURE 4

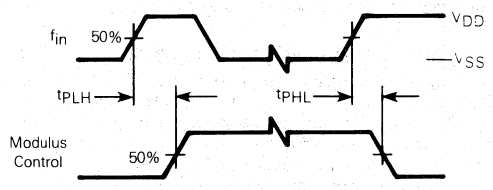


FIGURE 5

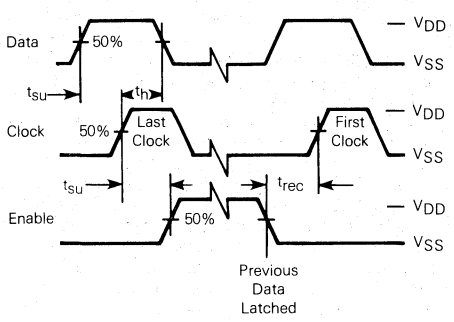


FIGURE 6

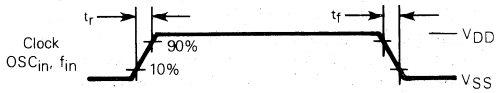


FIGURE 7

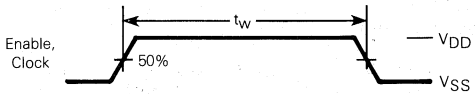
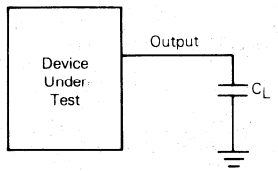


FIGURE 8 — TEST CIRCUIT



6

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For $V_{DD}=5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

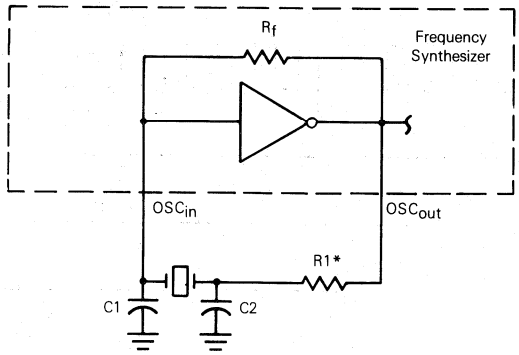
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

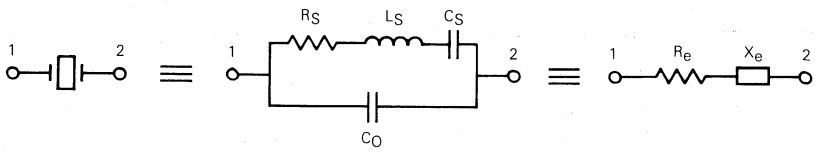
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES
OF THE AMPLIFIER

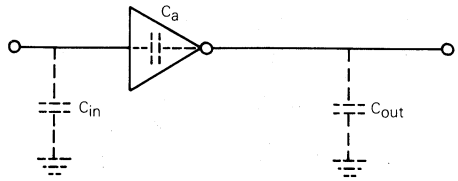
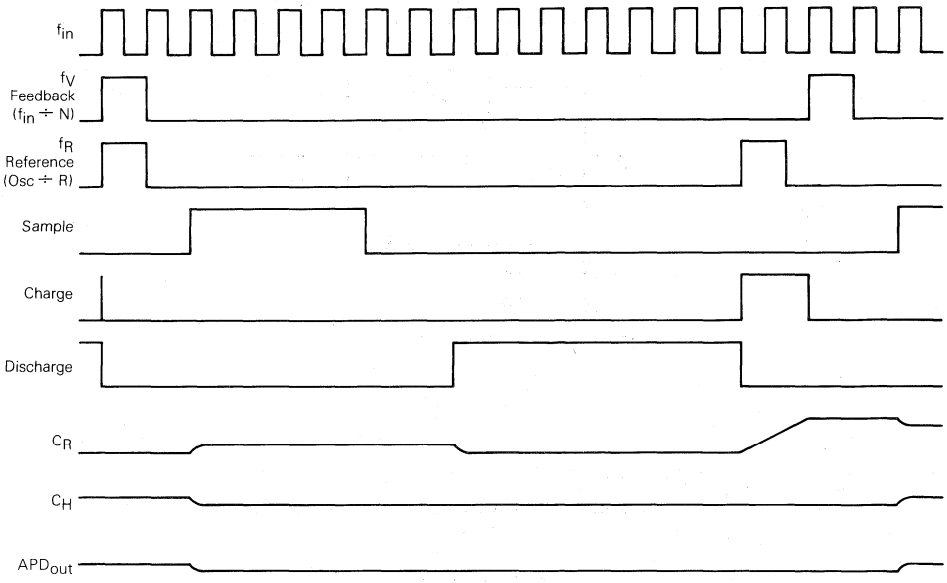


FIGURE 9 — TIMING DIAGRAM FOR MINIMUM DIVIDE VALUE (N = 16)



CMOS Remote Control Functions

7

CMOS REMOTE CONTROL FUNCTIONS

Device Number	Function
MC14457	Remote Control Transmitter
MC14458	Remote Control Receiver
MC14469	Addressable Asynchronous Receiver/Transmitter
MC14497	PCM Remote Control Transmitter
MC145026	Remote Control Encoder
MC145027	Remote Control Decoder
MC145028	Remote Control Decoder
MC145029	Remote Control Decoder

Function	Number of Address Bits	Number of Data Bits	Device Number	Number of Pins	Associated Device Number(s)
Transmitter	0	5*	**MC14457**	16	MC14458
Receiver	0	5*	**MC14458**	24	MC14457
Transmitter	0	6*	**MC14497**	18	MC3373
Encoder	Depends on Decoder	Depends on Decoder	**MC145026**	16	MC145027, MC145028, MC145029
Decoder	5	4	**MC145027**	16	MC145026
Decoder	9	0	**MC145028**	16	MC145026
Decoder	4	5	**MC145029**	16	MC145026
Addressable UART	7	7/8	**MC14469**	40	MC14469, MC6850

*These 5 or 6 bit codes specify commands or functions internal to the associated receiver devices.

MOTOROLA

MC14457
MC14458

MC14457 TRANSMITTER
MC14458 RECEIVER

The MC14457 and MC14458 are a transmitter and receiver pair constructed in CMOS monolithic technology. These units are designed for ultrasonic or infrared remote control of TV receivers, converters, communication receivers, and games. Selection of up to 16 channels may be done single entry; or up to 256 channels may be done double entry.

The MC14457 encodes each keyboard position into frequency-modulated biphase data. This transmitter functions with a 20- to 32-position keyboard and provides either channel select/toggle information (single-word transmission) or analog information (continuous transmission for the duration of key press). The MC14457 features low standby power between data transmissions.

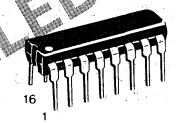
- Low External Component Count
- High Noise Immunity
- One Analog Output from Receiver
- Low Power
- Operating Voltage Range: 4.5 to 10.0 V for MC14457
  4.5 to 5.5 V for MC14458

CMOS MSI/LSI
(LOW-POWER COMPLEMENTARY MOS)

TRANSMITTER
RECEIVER

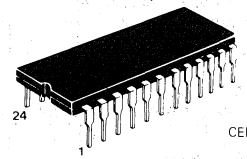
MC14457 TRANSMITTER

L SUFFIX
CERAMIC PACKAGE
CASE 620

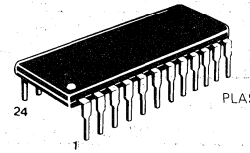


P SUFFIX
PLASTIC PACKAGE
CASE 648

MC14458 RECEIVER



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

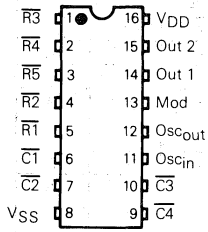
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14457	V_{DD}	−0.5 to +12	V
	MC14458		−0.5 to +6.0	
Input Voltage, All Inputs		V_{in}	−0.5 to V_{DD} + 0.5	V
DC Input Current, Per Pin		I_{in}	±10	mA
Operating Temperature Range		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−60 to +150	°C

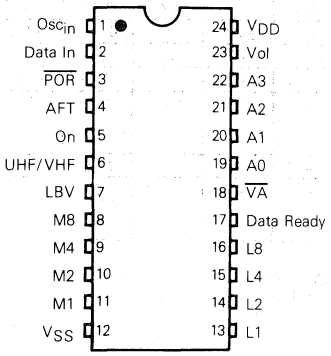
* Maximum Ratings are those values beyond which damage to the device may occur.

PIN ASSIGNMENTS

MC14457
TRANSMITTER



MC14458
RECEIVER



ORDERING INFORMATION

MC14XXX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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TRANSMITTER—MC14457

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$V_{in}=V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
$I_{out}=0\ \mu A$ "1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage # "0" Level	V_{IL}									V
(V_O=4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O=9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
"1" Level	V_{IH}									V
(V_O=0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O=1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
Output Drive Current — Pins 14, 15	I_{OH}									mA
(V_{OH}=2.5 V) Source		5.0	−6.0	–	−5.0	−9.0	–	−3.5	–	
(V_{OH}=9.5 V)		10	−3.2	–	−2.6	−4.5	–	−1.8	–	
(V_{OL}=2.5 V) Sink	I_{OL}	5.0	6.0	–	5.0	9.0	–	3.5	–	mA
(V_{OL}=0.5 V)		10	3.2	–	2.6	4.5	–	1.8	–	
Output Drive Current — Pin 13	I_{OH}									mA
(V_{OH}=4.6 V) Source		5.0	−0.26	–	−0.22	−0.44	–	−0.18	–	
(V_{OH}=9.5 V)		10	−0.6	–	−0.55	−1.12	–	−0.45	–	
(V_{OL}=0.4 V) Sink	I_{OL}	5.0	0.26	–	0.22	0.44	–	0.18	–	mA
(V_{OL}=0.5 V)		10	0.6	–	0.55	1.12	–	0.45	–	
Input Current — Pull-ups	I_{in}	10	–	–	50	500	1000	–	–	μA
Input Current — Pin 11	I_{in}	10	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current — Per Package	I_{DD}	5.0	–	50	–	0.008	50	–	375	μA
Osc_{in}=0 V, Other Inputs=Open, $I_{out}=0\ \mu A$		10	–	100	–	0.016	100	–	750	
Total Supply Current at an External Load Capacitance (C_L) of Figure 4 f=500 kHz (with any Analog command)	I_T	5.0	–	–	–	5.0	–	–	–	μA
		10	–	–	–	10	–	–	–	

RECEIVER—MC14458

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$V_{in}=V_{DD}$ or 0										
$I_{out}=0\ \mu A$ "1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage# "0" Level	V_{IL}									V
(V_O=4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O=0.5 or 4.5 V) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
Output Drive Current	I_{OH}									mA
(V_{OH}=2.5 V) Source		5.0	−0.5	–	−0.5	−1.7	–	−0.4	–	
(V_{OL}=0.4 V) Sink	I_{OL}	5.0	0.45	–	0.4	0.78	–	0.34	–	mA
Input Current (Osc_{in}, D_{in})	I_{in}	5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Current ($\overline{POR}$)	I_{in}	5.0	–	–	10	50	400	–	–	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, Per Package	I_{DD}	5.0	–	5.0	–	250	1000	–	–	μA
$\overline{POR}=V_{DD}$, Other Inputs=V_{DD} or 0, $I_{out}=0\ \mu A$										
Data Input Hysteresis	V_{Hys}	5.0	–	–	–	0.25	–	–	–	V
Total Supply Current at an External Load Capacitance (C_L) of Figure 6 f=500 kHz	I_T	5.0	–	–	–	400	–	–	–	μA

#Noise immunity specified for worst-case input combination
Noise Margin for both "1" and "0" level=1.0 V min @ V_{DD}=5.0 V
2.0 V min @ V_{DD}=10 V

SWITCHING CHARACTERISTICS (MC14457 – Transmitter, V_{DD} = 5 to 15 V; MC14458 – Receiver, V_{DD} = 5 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rise and Fall Time – Receiver C_L = 100 pF	t_{TLH}, t_{THL}	–	0.3	1.0	μs
Oscillator Start-Up Time – Transmitter	t_{on}	–	8.0	–	μs
Clock Pulse Frequency	PRF	–	1500	600	kHz

MC14457 – TRANSMITTER

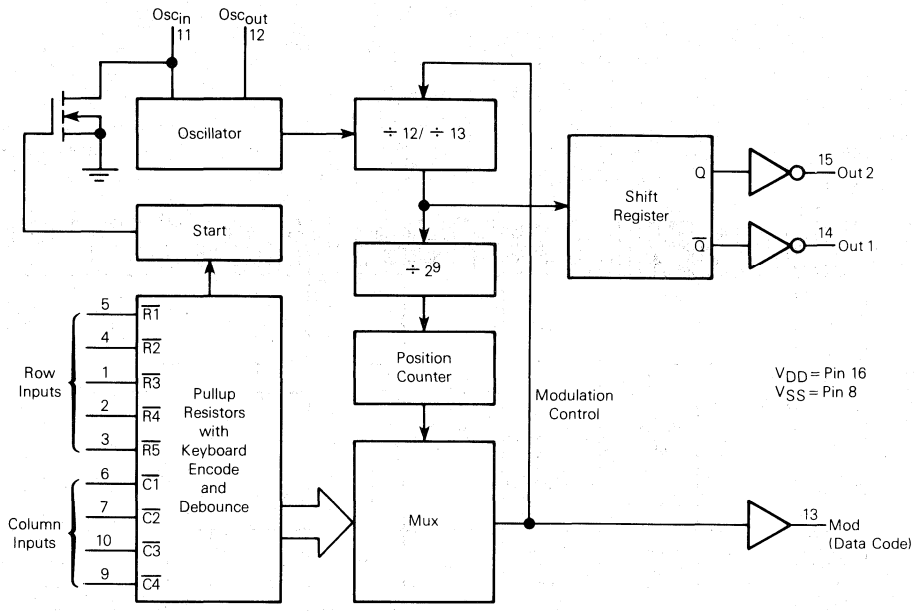

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FIGURE 1 — EXAMPLE OF TRANSMITTED WORD

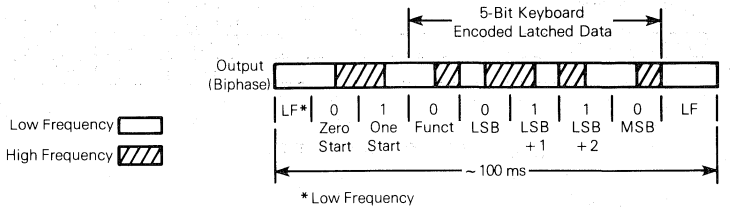
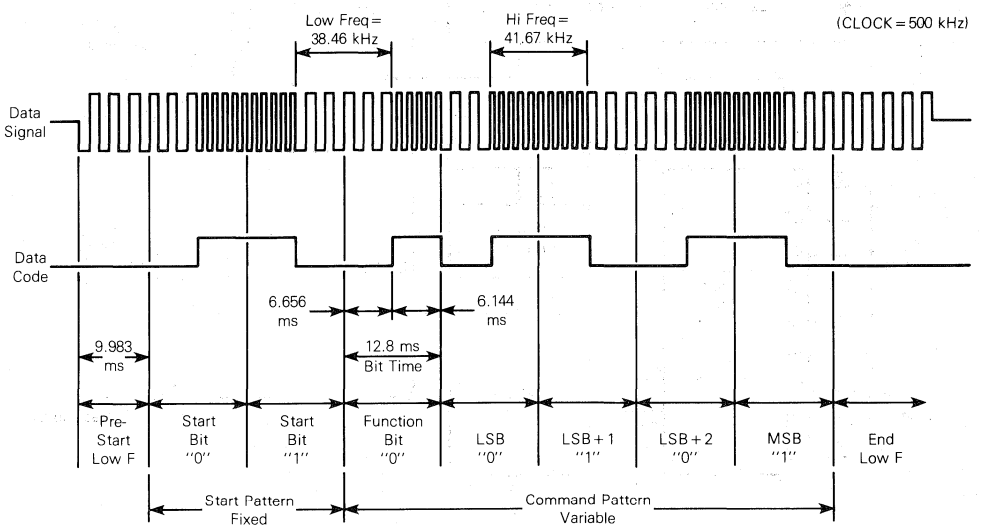


FIGURE 2 — DATA SIGNAL



MC14457 TRANSMITTER PIN DESCRIPTIONS

$\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$, $\overline{R5}$, ROW INPUTS (PINS 5, 4, 1, 2, 3) — These pins are the row inputs and are active in the low state. On-chip pullup resistors are provided on each of these inputs.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, COLUMN INPUTS (PINS 6, 7, 10, 9) — These pins are the column inputs and are active in the low state. On-chip pullup resistors are provided on each of these inputs.

Out 1, Out 2, OUTPUTS (PINS 14, 15) — These pins provide push-pull output and can be used with ceramic transducers or LEDs. In the non-operating condition, both outputs are at ground potential.

Osc_{in}, Osc_{out}, OSCILLATORS (PINS 11, 12) — These pins are the input/output terminals of the oscillator. They can be used with a ceramic resonator or crystal. The oscillator is automatically turned off after the data is transmitted for low current quiescent operation.

If an external oscillator is used, a current limiting resistor should be added, due to the presence of an internal pull-down device on the oscillator input.

Mod, MODULATION (PIN 13) — This pin is a data code output. Note that there is no power-up reset.

TABLE 1 — DATA CODE

Key Number	Operation	Row (Active Low)	Column (Active Low)	Transmitter Data and Receiver Output Address					$\overline{VA}$ Pulse	Notes
				MSB/A3	LSB+2/A2	LSB+1/A1	LSB/A0	Function*		
1	Digit 0	R1	C1	0	0	0	0	0	–	1
2	Digit 1	R1	C2	0	0	0	1	0	–	1
3	Digit 2	R2	C1	0	0	1	0	0	–	1
4	Digit 3	R2	C2	0	0	1	1	0	–	1
5	Digit 4	R3	C1	0	1	0	0	0	–	1
6	Digit 5	R3	C2	0	1	0	1	0	–	1
7	Digit 6	R4	C1	0	1	1	0	0	–	1
8	Digit 7	R4	C2	0	1	1	1	0	–	1
9	Digit 8	R5	C1	1	0	0	0	0	–	1
10	Digit 9	R5	C2	1	0	0	1	0	–	1
11	Chan. Search ↓	R1	C3	0	0	0	0	1	↙	2
12	Chan. Search ↑	R1	C4	0	0	0	1	1	↙	2
13	Fine Tuning ↓	R2	C3	0	0	1	0	1	↙	3
14	Fine Tuning ↑	R2	C4	0	0	1	1	1	↙	3
15	Spare	R3	C3	0	1	0	0	1	↙	3
16	Spare	R3	C4	0	1	0	1	1	↙	3
17	Volume ↓	R4	C3	0	1	1	0	1	↙	3
18	Volume ↑	R4	C4	0	1	1	1	1	↙	3
19	Mute on/off	R5	C3	1	0	0	0	1	↙	2
20	Off	R5	C4	1	0	0	1	1	↙	2
21	Digit 10	R2•R5	C1	1	0	1	0	0	–	1
22	Digit 11	R2•R5	C2	1	0	1	1	0	–	1
23	Digit 12	R3•R5	C1	1	1	0	0	0	–	1
24	Digit 13	R3•R5	C2	1	1	0	1	0	–	1
25	Digit 14	R2•R3•R5	C1	1	1	1	0	0	–	1
26	Digit 15	R2•R3•R5	C2	1	1	1	1	0	–	1
27	Spare	R2•R5	C3	1	0	1	0	1	↙	3
28	Spare	R2•R5	C4	1	0	1	1	1	↙	3
29	Spare	R3•R5	C3	1	1	0	0	1	↙	3
30	Spare	R3•R5	C4	1	1	0	1	1	↙	3
31	Spare	R2•R3•R5	C3	1	1	1	0	1	↙	3
32	Spare	R2•R3•R5	C4	1	1	1	1	1	↙	3

Notes:
1. Channel Select Keys (Function Bit=0). Data is transmitted once each time a key is activated.
2. Toggling type On/Off or counter advance type keys. Data is transmitted once each time a key is activated.
3. Analog Up/Down or On/Off keys, i.e., one key for Down or Off and another key for Up or On. Data transmission is repeated as long as the key is operated.

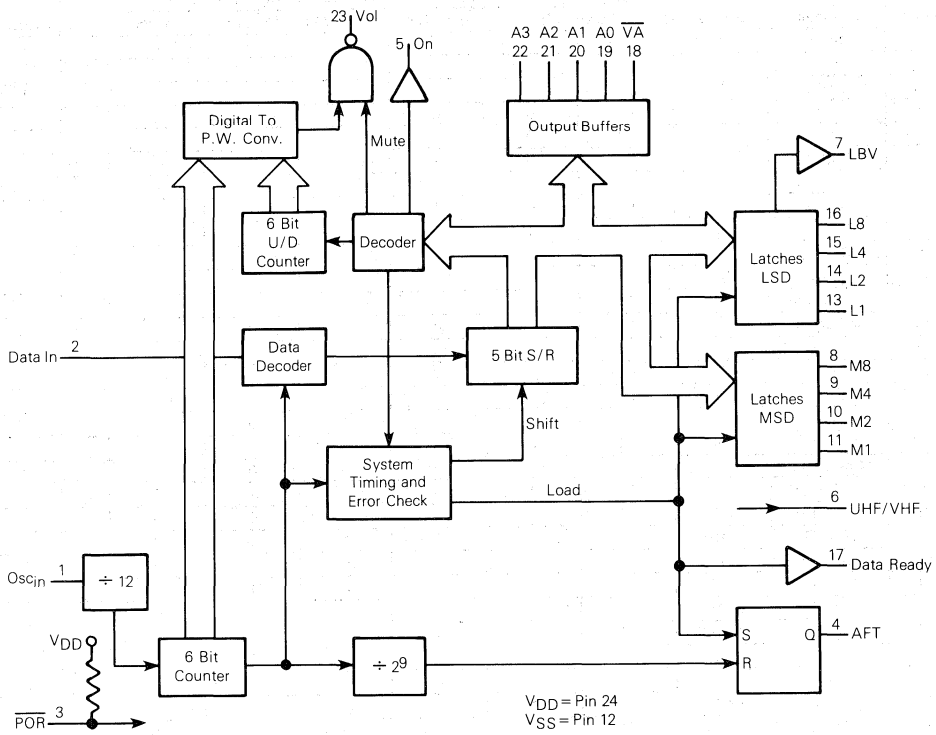
*The function bit is used only internally by the MC14458 receiver as a steering bit.

In Table 1, all channel select data is noted by the function bit equal to zero. For functions other than channel, the function bit equals one.

The four toggling or counter advance type keys that transmit data once each time a key is activated are Mute, Off, Channel Search Up, and Channel Search Down.

The twelve remaining analog keys (Vol, Tint, Color, etc.) transmit data as long as the key is activated. The keys' functions are arranged to provide the most typical application without grounding of multiple row or columns required.

MC14458 — RECEIVER



7

MC14458 RECEIVER PIN DESCRIPTIONS

Data In, DATA INPUT (PIN 2) — The amplified ultrasonic data signal (after amplification and limiting forms a square wave with a peak-to-peak value of V_{DD}) is applied to this input terminal.

Osc$_{in}$, OSCILLATOR INPUT (PIN 1) — The oscillator input pin of the receiver is connected to an oscillator that provides, for example, a 500 kHz square wave signal. A typical oscillator circuit is shown in Figure 5. Accuracy of one percent, relative to the oscillator frequency in the transmitter, is recommended for satisfactory performance in very high echo producing environments.

L1, L2, L4, L8, M1, M2, M4, M8, CHANNEL OUTPUTS (PINS 13, 14, 15, 16, 11, 10, 9, 8) — The eight data output pins provide latched data corresponding to the channel selected on the transmitter keyboard. L1 through L8 are the least significant bits; M1 through M8 are the most significant bits. The data on these pins is accompanied by a Data Ready signal.

Data Ready, DATA READY SIGNAL (PIN 17) — A positive pulse with a duration of 768 μs appears at Pin 17 of the receiver approximately 0.1 second after a complete command is entered on the remote control transmitter keyboard. The negative going edge of this pulse may be used for triggering purposes.

NOTE: A complete command is one digit in the single entry mode or two digits in the double entry mode.

AFT, AUTOMATIC FINE TUNING ENABLE (PIN 4) — The voltage level at this pin is low for a time duration of 0.393 seconds following a change in selected channel to allow disabling the tuner AFT circuit. Also, miscellaneous commands 0000, 0001, 0010, and 0011 (Channel Search Up/Down, Fine Tuning Up/Down) will cause this disable feature.

$\overline{\text{POR}}$, POWER-ON RESET (PIN 3) — This pin is low for power-on reset of the analog output to 0 pulse width and off/on output to 0. An internal pull-up device delivers 10 to 400 μA to charge an external capacitor. Reset occurs until the input voltage reaches 70 percent V_{DD}. All internal registers will also be reset.

A0, A1, A2, A3, ADDRESS OUTPUTS (PINS 19, 20, 21, 22) — The address outputs of the receiver identify selected analog and on/off commands for use in system expansion. The data on these lines is valid when accompanied by a Valid Address pulse.

$\overline{VA}$, VALID ADDRESS (PIN 18) — A negative going pulse with a duration of 768 μs appears at Pin 18 approximately 0.1 seconds after an analog on/off key on the remote control transmitter keyboard is operated. Either edge of this pulse may be used for control of add-on circuits.

The Valid Address pulse is repeated every 102.4 ms for as long as a key is operated which provides repeated transmission of data when held down.

The Valid Address signal may be used in conjunction with the Address Outputs to drive memories to provide additional control functions such as color, tint, etc.

The Valid Address pulse may be used to provide a stepping clock for up/down counters in a memory. The least significant address line (A0) is used to identify the up or down mode, and the remaining address lines (A1, A2, A3) are decoded to enable each individual control circuit.

By adding up/down counters to the Data Outputs, it is possible to use the Valid Address pulse and a decoded address for implementing a channel up/down stepping function from the remote control. Additional On/Off functions may be obtained by using the Valid Address pulse in combination with a decoded address for setting and resetting of latches. The Valid Address signal is disabled in the standby mode (ON output at logical 0).

UHF/VHF, ULTRA HIGH FREQUENCY/VERY HIGH FREQUENCY OUTPUT (PIN 6) — This pin of the receiver provides a low level when the selected channel is a VHF channel (00 to 13, or 84 to 99). A high level on Pin 6 identifies selection of a UHF channel (14 to 83). This signal is provided to permit switching of VHF and UHF tuners.

On, ON (PIN 5) — This pin of the receiver provides a low level following operation of the Off command (1001) on the remote-control transmitter. The signal on this pin changes to a high level when a channel is selected.

Vol, VOLUME CONTROL (PIN 23) — An analog output voltage in the range between 0 V and V_{DD} is obtained by integrating the signal at the Vol pin through a low-pass filter. The analog voltage resolution has been chosen to be 64 steps. The value can be incremented or decremented in steps of one by keys providing commands 0111 and 0110, respectively (see Table 1).

This analog voltage can be varied up or down at a speed of approximately 10 steps per second. The D/A conversion is performed with an underflow and an overflow limiting circuit. The Vol pin is normally used for the control of volume. The first time power is applied to the remote-control receiver, the volume output is 0 volts.

The Vol signal may be increased after a channel has been selected by operating the key providing a command 0111 (Volume Up).

The Vol signal may be muted by operating a key on the transmitter providing command 1000. Return to the original output prior to muting may be achieved by operating the mute key a second time or by operating the volume-up key.

In the muted mode, the analog level is memorized and cannot be varied by the up/down controls on the transmitter.

LBV, LOW BAND (PIN 7) — This pin will go HIGH whenever channels 02, 03, 04, 05, or 06 are selected. The output is LOW for channels 00, 01, and 07 through 99.

OPERATION

The receiver can be placed in a single-digit mode of operation by connecting the M4 data output (Pin 9) to V_{DD} and the UHF output (Pin 6) to V_{SS}. In this mode, the L1 through L8 channel outputs will change immediately after the entry of a single digit on the transmitter keys. The M1 through M8 outputs are not used in this mode (see Figure 6).

As one example of operation, a free-running ceramic resonator oscillator (at 500 kHz), triggered by the depression of any key, is divided by 12 or 13 to provide frequencies of 41.67 or 38.46 kHz. The transmitted data "zero" consists of 256 periods of the lower frequency followed by an equal number of the higher frequency. Mark to space ratio is kept at 1:1 in each case. A data "one" reverses the order of the two frequencies.

Row and column information from the keyboard is encoded into a 5-bit word and loaded onto data latches on the edge of transmit enable. This data, preceded by two bits, 0 and 1, is used in sequence to provide biphase control of the divider and, consequently, the bit pattern transmitted from the unit. Each 7-bit word begins and ends with a low frequency burst. Operation of a channel select key produces an output data stream for a duration of approximately 100 ms.

APPLICATIONS INFORMATION

Typical circuits for the transmitter and receiver chips are shown in Figures 3 through 7.

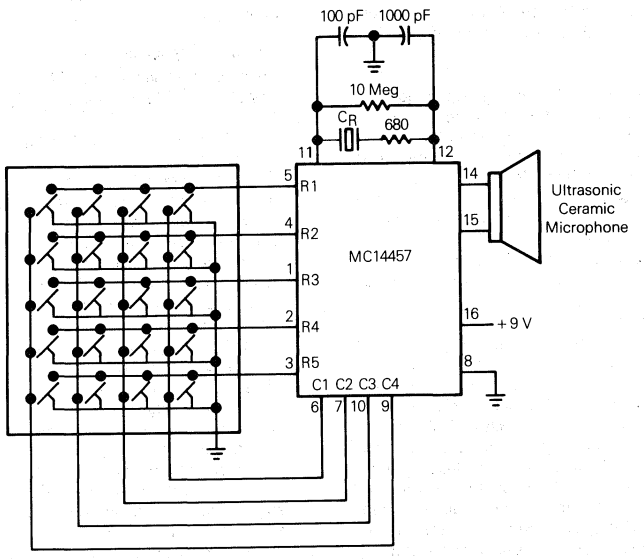
The transmitters, with the keyboard shown, transmit the first twenty codes from Table 1. The circuits of Figure 3 transmit via ultrasonic; whereas, the circuit of Figure 4 transmits infrared light. In Figure 3, a push-pull output at Pins 14 and 15 allows a balance drive to the ceramic microphone, which virtually doubles the transmitted power, compared to a single-ended output.

The diagram in Figure 5 shows an amplifier connected to a remote receiver. The bias resistor (photodiode) of the amplifier requires bias. The bias voltage is determined by the choice of photodiode and system considerations such as ambient light. Most of the required gain is realized using three of the hex inverters in the MC14069UB package. A fourth inverter from the same package operates a 500 kHz oscillator circuit.

Figure 6 shows a block diagram of a PLL system. The receiver directly addresses a synthesizer. In this diagram, a complete command consists of two channel digits followed by an Enter code. The Enter code into the synthesizer is a 0101 in complementary logic. The transmitted code from the transmitter is 1010, which is Function 10 from Table 1.

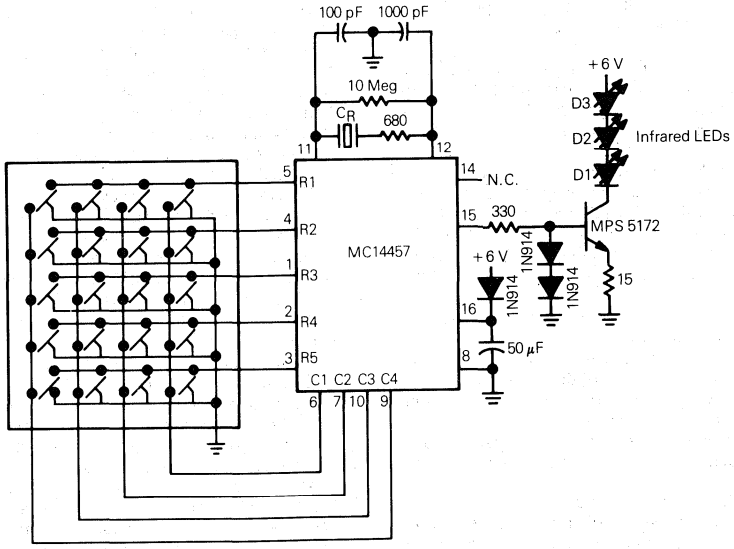
A block diagram of a tuning address system is shown in Figure 7. This block diagram incorporates a one-chip microcomputer that would be programmed to the system's needs. The system can be expanded up to 256 channels.

FIGURE 3 — TYPICAL ULTRASONIC SYSTEM



Note: C_R is a ceramic resonator, Radio Materials Corp. type CR30 or equivalent.

FIGURE 4 — TYPICAL INFRARED SYSTEM



Note: C_R is a ceramic resonator, Radio Materials Corp. type CR30 or equivalent.

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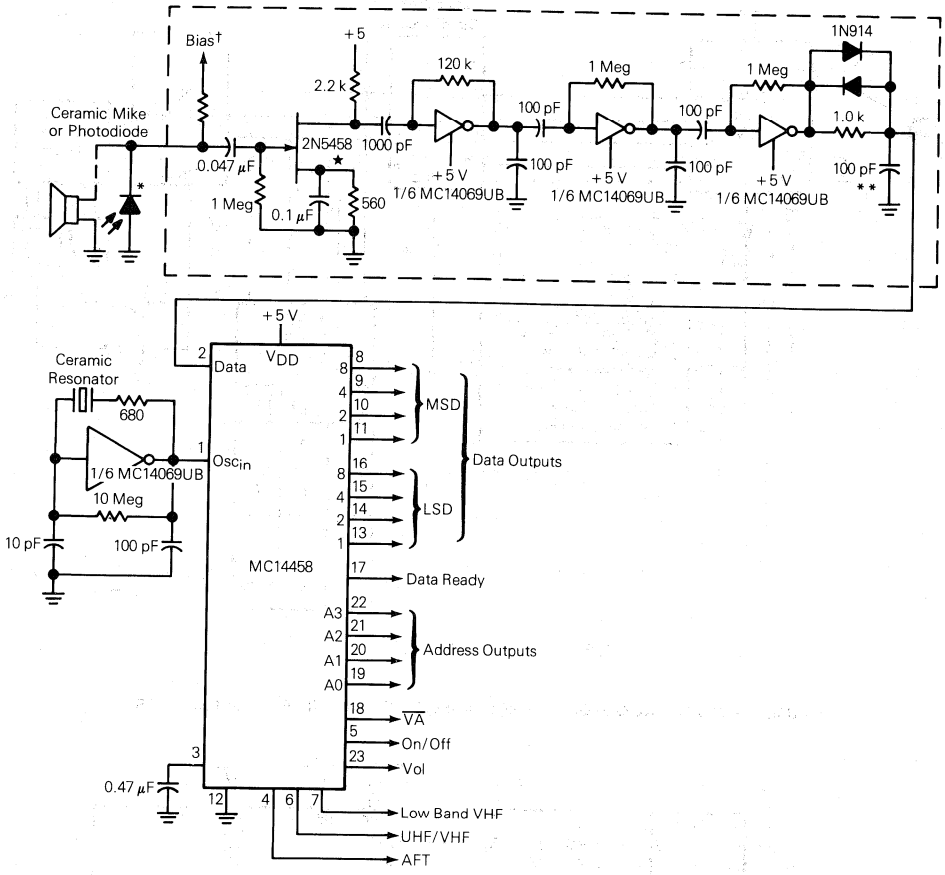
FIGURE 5 — TYPICAL REMOTE CONTROL RECEIVER CIRCUIT DIAGRAM



NOTES:

†Bias used for photodiode only.
*It is mandatory to use an infrared filter in front of the photodiode. Type Kodak 87C or similar.
★Select 2N5458 FETs with an I_{DSS} of 2 to 4 mA.
**100 pF capacitor should be placed as close as possible to Pin 2 of the MC14458.

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FIGURE 6 — BLOCK DIAGRAM OF A PLL SYSTEM

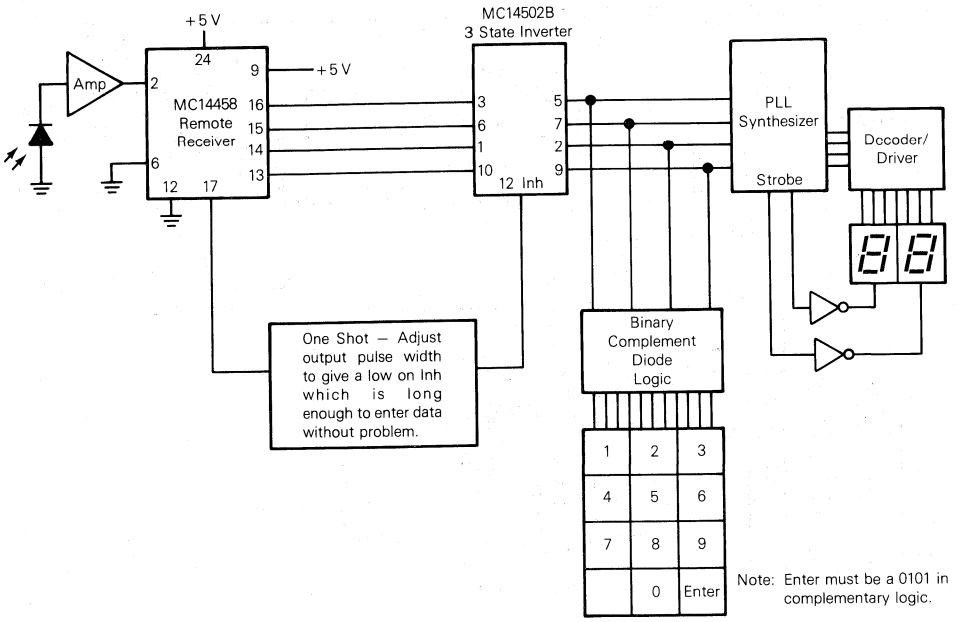
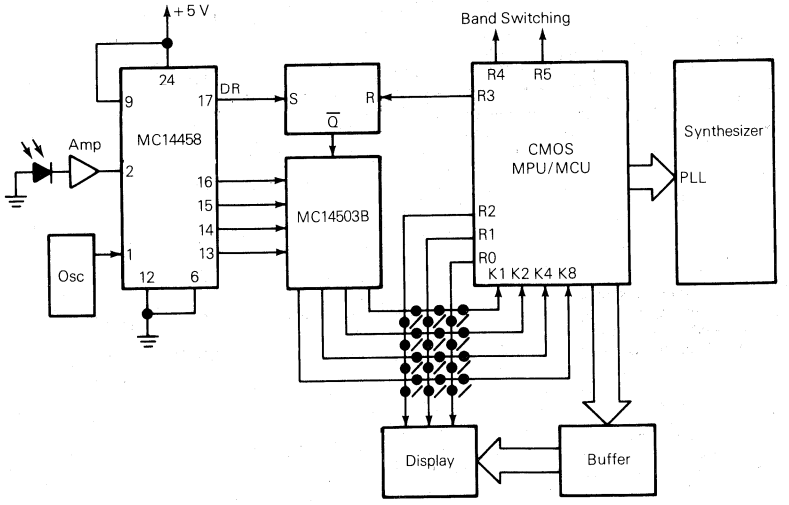


FIGURE 7 — BLOCK DIAGRAM OF A TUNING ADDRESS SYSTEM FOR UP TO 256 CHANNELS



MOTOROLA

MC14469

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER

The MC14469 Addressable Asynchronous Receiver Transmitter is constructed with MOS P-channel and N-channel enhancement devices in a single monolithic structure (CMOS). The MC14469 receives one or two eleven-bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 will then transmit its information in two eleven-bit-word data streams. Each of the transmitted words contains eight data bits, even parity bit, start and stop bit.

The received word contains seven address bits and the address of the MC14469 is set on seven pins. Thus 2^7 or 128 units can be interconnected in simplex or full duplex data transmission. In addition to the address received, seven command bits may be received for data or control use.

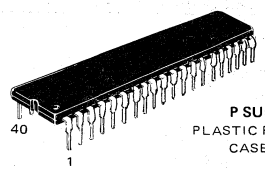
The MC14469 finds application in transmitting data from remote A-to-D converters, remote MPUs or remote digital transducers to the master computer or MPU.

- Supply Voltage Range — 4.5 Vdc to 18 Vdc
- Low Quiescent Current — 75 μAdc maximum @ 5 Vdc
- Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
- Receive — Serial to Parallel
  Transmit — Parallel to Serial
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator
- See also Application Note AN-806

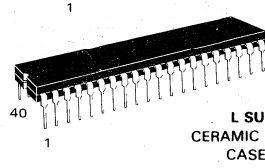
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER



P SUFFIX
PLASTIC PACKAGE
CASE 711

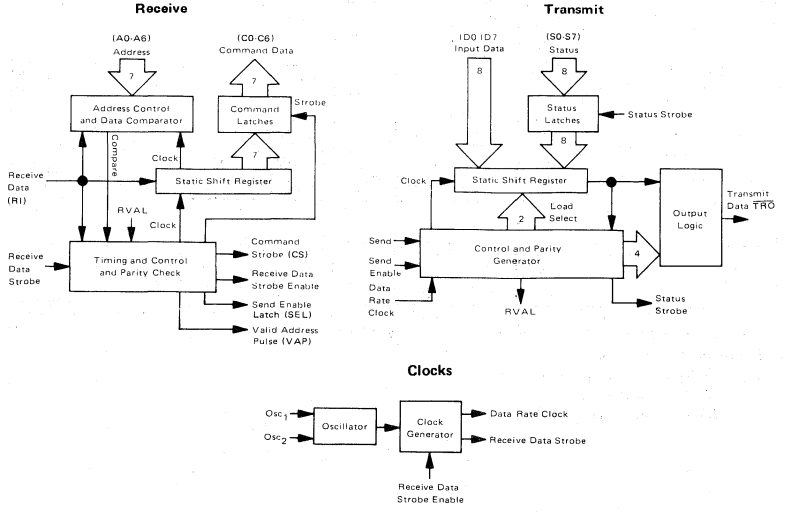


L SUFFIX
CERAMIC PACKAGE
CASE 734

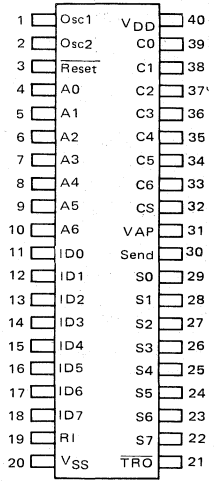
ORDERING INFORMATION

MC14xxx — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package

BLOCK DIAGRAMS



PIN ASSIGNMENTS



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MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 20.

	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

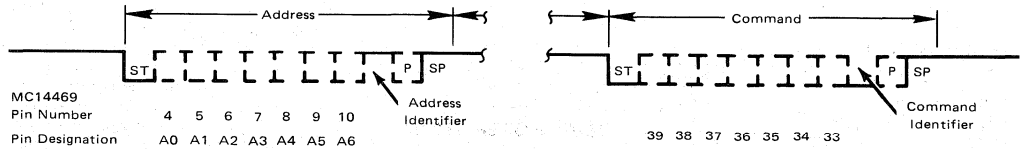
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95		14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (Except Pin 2)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.35	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current (Pin 2 Only)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.19	–	-0.16	-0.32	–	-0.13	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.04	–	-0.035	-0.07	–	-0.03	–	
(V_{OH} = 9.5 Vdc)		10	-0.09	–	-0.08	-0.16	–	-0.06	–	
(V_{OH} = 13.5 Vdc)		15	-0.29	–	-0.27	-0.48	–	-0.2	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.1	–	0.085	0.17	–	0.07	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.17	–	0.14	0.28	–	0.1	–	
(V_{OL} = 1.5 Vdc)		15	0.50	–	0.42	0.84	–	0.3	–	
Maximum Frequency	f_{max}	4.5	400	–	365	550	–	310	–	kHz
Input Current	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Pull-Up Current (Pins 4-18)	I_{UP}	15	12	120	10	50	100	8.0	85	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	75	–	0.010	75	–	565	μAdc
(Per Package)		10	–	150	–	0.020	150	–	1125	
		15	–	300	–	0.030	300	–	2250	
Supply Voltage	V_{DD}	–	+4.5	+18.0	+4.5	–	+18.0	+4.5	+18.0	Vdc

Noise immunity specified for worst-case input combination.
Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

DATA FORMAT AND CORRESPONDING DATA POSITION AND PINS FOR MC14469 AND MC6850

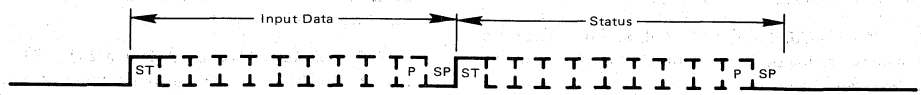
RECEIVE DATA (RI; Pin 19)



MC14469							
Pin Number	4	5	6	7	8	9	10
Pin Designation	A0	A1	A2	A3	A4	A5	A6
MC6850							
ACIA Pin Number	22	21	20	19	18	17	16
Pin Designation	D0	D1	D2	D3	D4	D5	D6

Pin Number	39	38	37	36	35	34	33
Pin Designation	C0	C1	C2	C3	C4	C5	C6
ACIA Pin Number	22	21	20	19	18	17	16
Pin Designation	D0	D1	D2	D3	D4	D5	D6

TRANSMIT DATA ($\overline{TRO}$; Pin 21)



MC14469								
Pin Numbers	11	12	13	14	15	16	17	18
Pin Designation	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7
MC6850								
ACIA Pin Number	22	21	20	19	18	17	16	15
Pin Designation	D0	D1	D2	D3	D4	D5	D6	D7

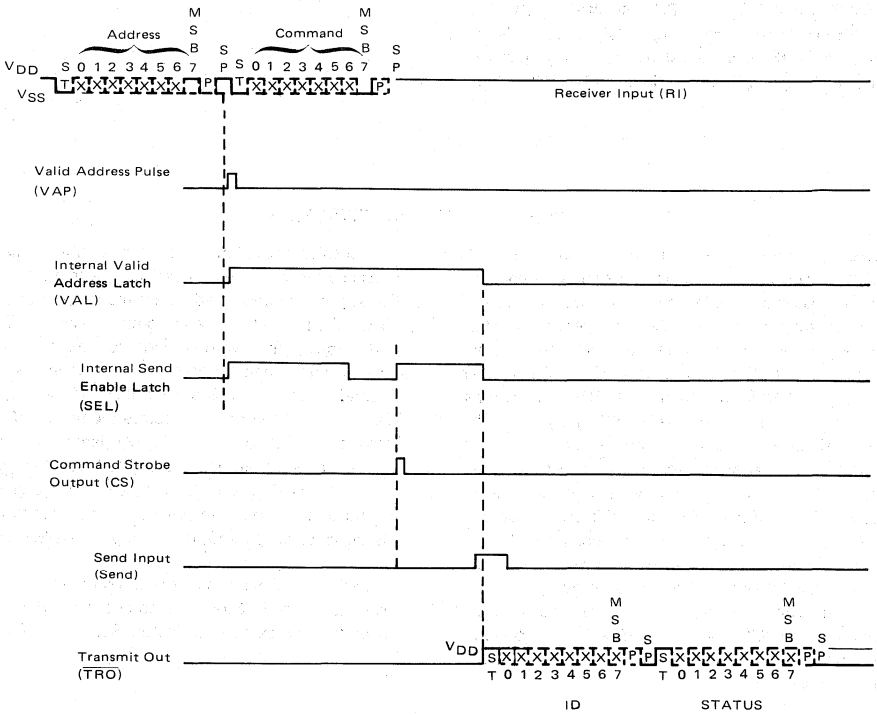
Pin Numbers	29	28	27	26	25	24	23	22
Pin Designation	S0	S1	S2	S3	S4	S5	S6	S7
ACIA Pin Number	22	21	20	19	18	17	16	15
Pin Designation	D0	D1	D2	D3	D4	D5	D6	D7

ST = Start Bit
P = Parity Bit
SP = Stop Bit

A0 → A6 = Address Bits
C0 → C6 = Command Bits
D0 → D7 = ACIA Bus Bits

ID0 → ID7 = MC14469 Identification Code
S0 → S7 = MC14469 Status Code

TYPICAL RECEIVE/SEND CYCLE



DEVICE OPERATION

OSCILLATOR (Osc1, Osc2; Pins 1, 2) – These pins are the oscillator input and output. (See Figure 1.)

RESET ($\overline{\text{Reset}}$; Pin 3) – When this pin is pulled low, the circuit is reset and ready for operation.

ADDRESS (A0-A6; Pin 4, 5, 6, 7, 8, 9, 10) – These are the address setting pins which contain the address match for the received signal.

INPUT DATA (ID0-ID7; Pins 11, 12, 13, 14, 15, 16, 17, 18) – These pins contain the input data for the first eight bits of data to be transmitted.

RECEIVE INPUT (RI; Pin 19) – This is the receive input pin.

NEGATIVE POWER SUPPLY (V_{SS}; Pin 20) – This pin is the negative power supply connection. Normally this pin is system ground.

TRANSMIT REGISTER OUTPUT SIGNAL ($\overline{\text{TRO}}$; Pin 21) – This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

SECOND or STATUS INPUT DATA (S0-S7; Pins 22, 23, 24, 25, 26, 27, 28, 29) – These pins contain the input data for the second eight bits of data to be transmitted.

SEND (Send; Pin 30) – This pin accepts the send command after receipt of an address.

VALID ADDRESS PULSE (VAP; Pin 31) – This is the output for the valid address pulse upon receipt of a matched incoming address.

COMMAND STROBE (CS; Pin 32) – This is the output for the command strobe signifying a valid set of command data on pins 33-39.

COMMAND WORD (C0-C6; Pins 33, 34, 35, 36, 37, 38, 39) – These pins are the readout of the command word which is the second word of the received signal.

POSITIVE POWER SUPPLY (V_{DD}; Pin 40) – This pin is the package positive power supply pin.

7

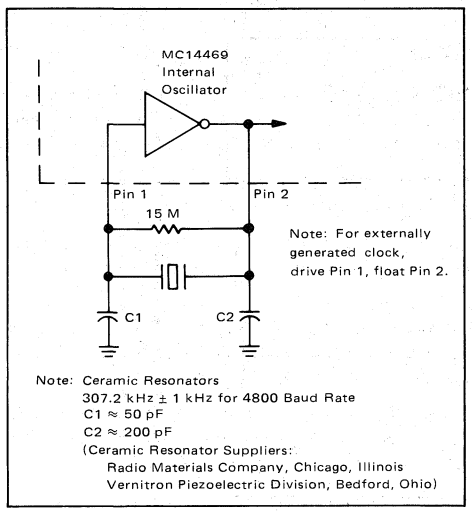
OPERATING CHARACTERISTICS

The receipt of a start bit on the Receive Input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (A0-A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word "1" or a command word "0". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address compared, a Valid Address Pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit and a stop bit. The eight data bits are composed of a seven-bit command, and a "0" which indicates a command word. At the end of the command word a Command Strobe Pulse (CS) occurs.

A positive transition on the Send input initiates the transmit sequence. Send must occur within 7 bit times of CS. Again the transmitted data is made up of two eleven-bit words, i.e., address and command words. The data portion of the first word is made up from Input Data inputs (ID0-ID7), and the data for the second word from Second Input Data (S0-S7) inputs. The data on inputs ID0-ID7 is latched one clock before the falling edge of the start bit. The data on inputs S0-S7 is latched on the rising edge of the start bit. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines. $\overline{\text{TRO}}$ begins either ½ or 1½ bit times after Send, depending where Send occurs.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. Pin 1 may be driven from an external oscillator. See Figure 1.

FIGURE 1 – OSCILLATOR CIRCUIT



Note: Ceramic Resonators
307.2 kHz ± 1 kHz for 4800 Baud Rate
C1 ≈ 50 pF
C2 ≈ 200 pF
(Ceramic Resonator Suppliers:
Radio Materials Company, Chicago, Illinois
Vernitron Piezoelectric Division, Bedford, Ohio)

FIGURE 2 – RECTIFIED POWER FROM DATA LINES CIRCUIT

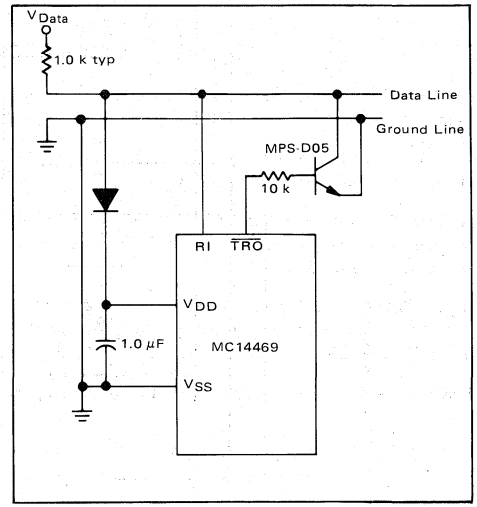
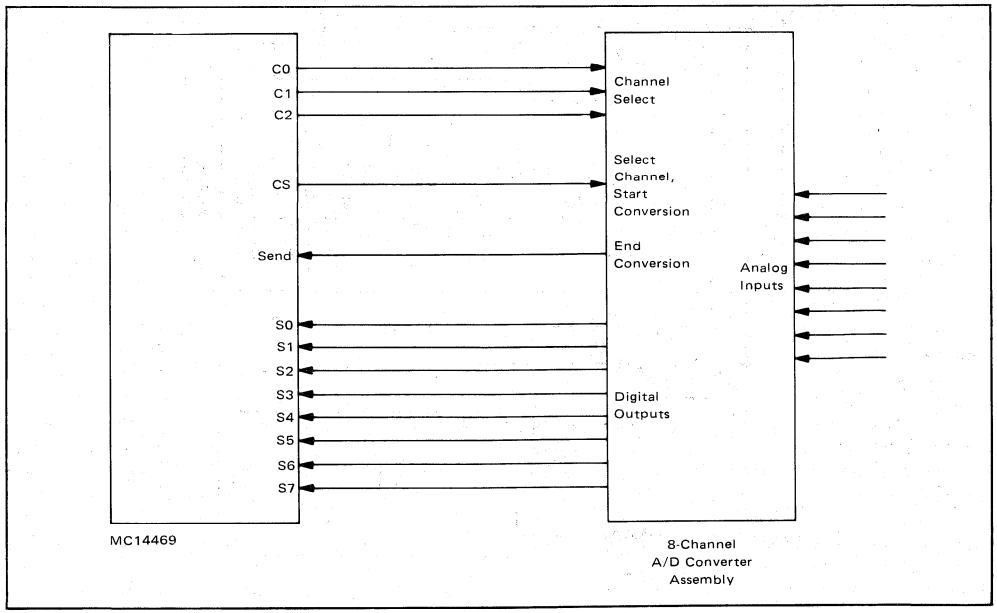


FIGURE 3 – A-D CONVERTER INTERFACE



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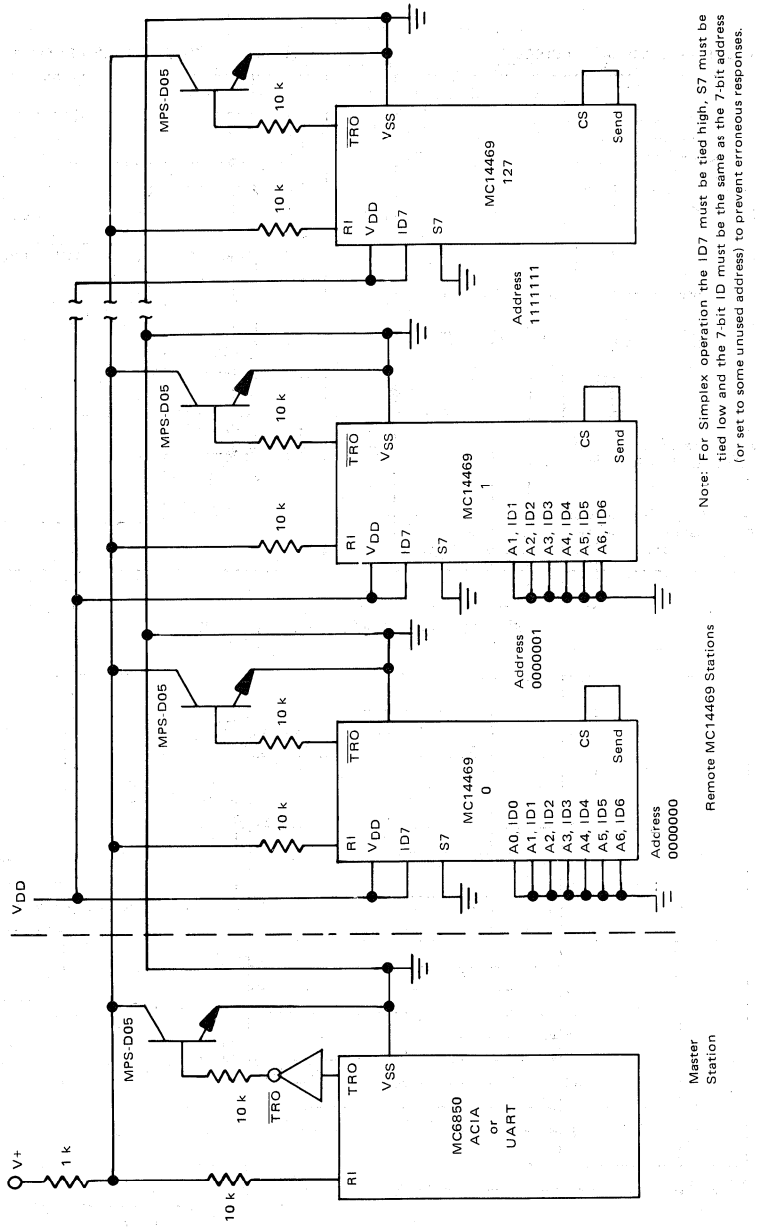


FIGURE 4 – SINGLE LINE, SIMPLEX DATA TRANSMISSION

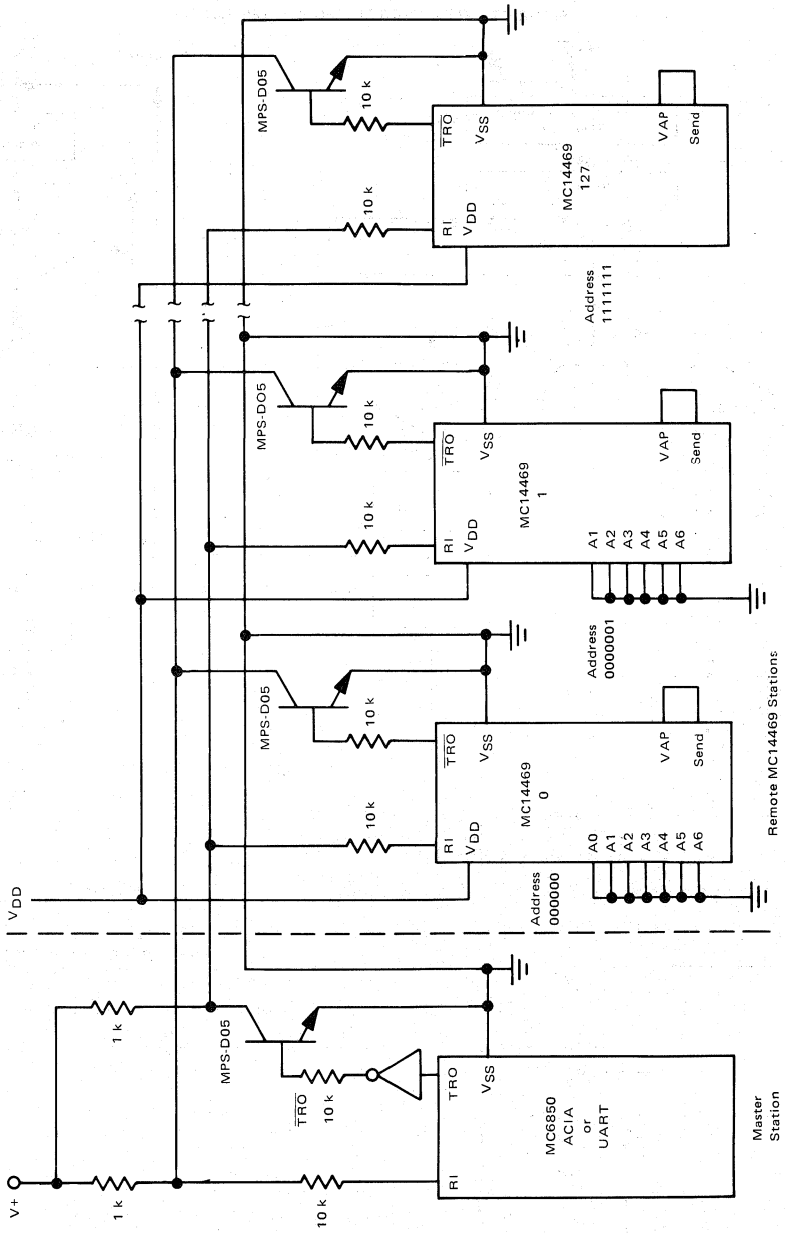
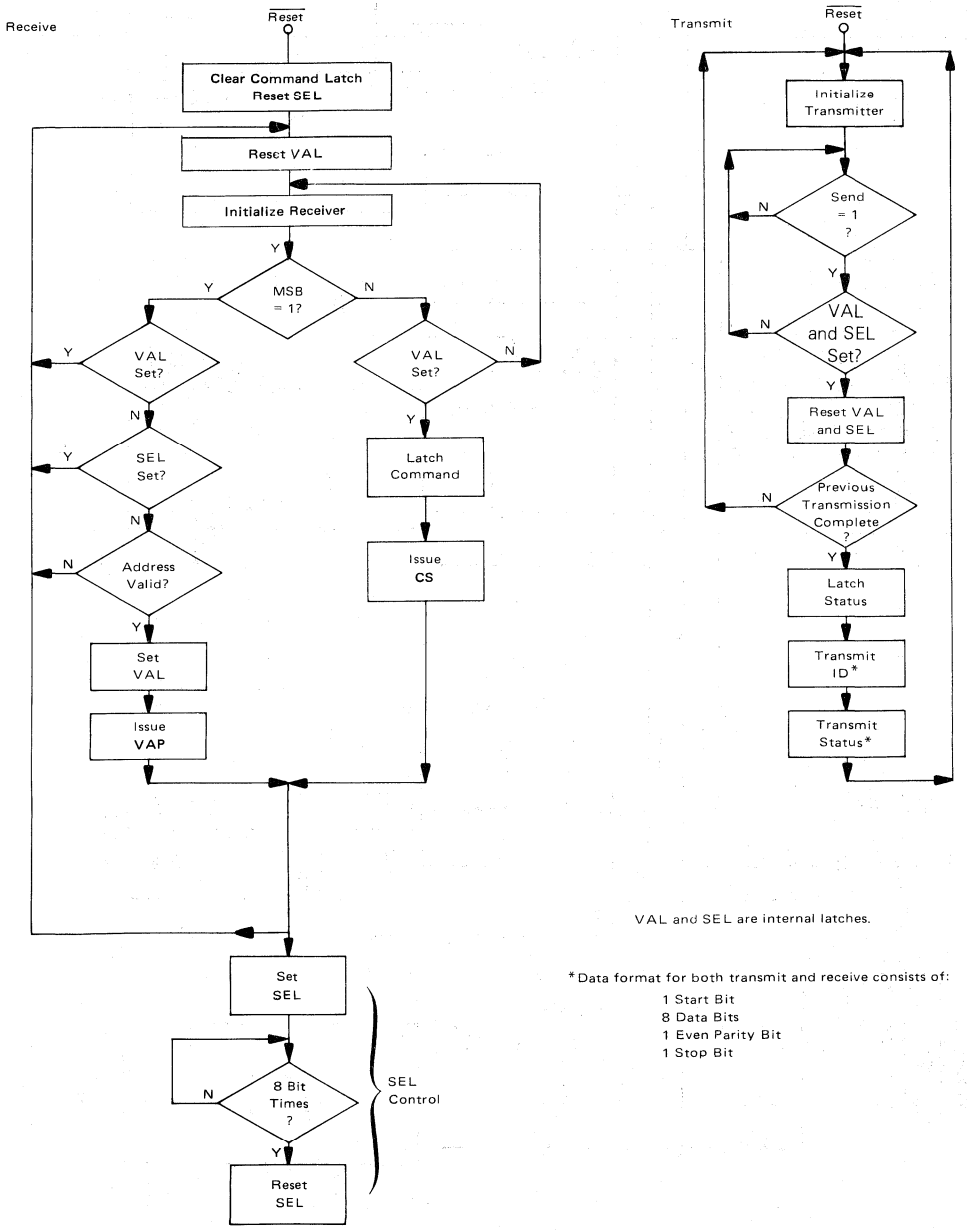


FIGURE 5 – DOUBLE LINE, FULL DUPLEX DATA TRANSMISSION

7

FIGURE 6 – FLOW CHART OF MC14469 OPERATION



VAL and SEL are internal latches.

*Data format for both transmit and receive consists of:

1 Start Bit
8 Data Bits
1 Even Parity Bit
1 Stop Bit

7

MOTOROLA

MC14497

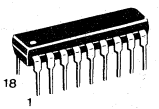
PCM REMOTE CONTROL TRANSMITTER

The MC14497 is a PCM remote control transmitter realized in CMOS technology. Using a dual-single (FSK/AM) frequency biphase modulation, the transmitter is designed to work with the MC3373 receiver.

- Both FSK/AM Modulation Selectable
- 62 Channels – Up to 62 Keys
- 500 kHz Reference Oscillator Controlled by Inexpensive Ceramic Resonator
- Very Low Duty Cycle
- Very Low Standby Current
- Infrared Transmission
- Selectable Start-Bit Polarity (AM only)
- Shifted Key Mode Available
- Wide Operating Voltage Range: 4 to 10 Volts

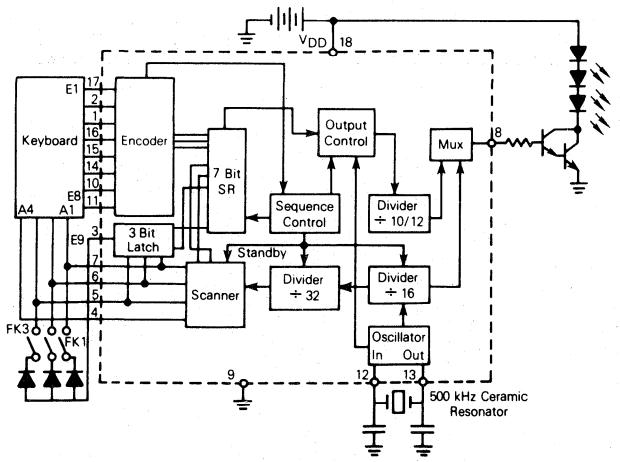
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

PCM REMOTE CONTROL TRANSMITTER

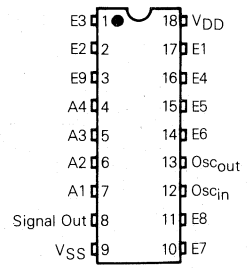


P SUFFIX
PLASTIC PACKAGE
CASE 707

FIGURE 1 – BLOCK DIAGRAM



PIN ASSIGNMENT



7

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A=0 to 70°C; all Voltages Referenced to V_{SS})

Characteristic		Symbol	Pin	V_{DD}	Min	Max	Unit
Supply Voltage		V_{DD}	18	–	4.0	10.0	V
Supply Current		I_{DD}	18				
Idle				10	–	50	μA
Operation				10	–	5	mA
Output Current – Signal			8				μA
V_{OH}=3.0 V	Source	I_{OH}		4	−900	–	
V_{OL}=0.5 V	Sink	I_{OL}		4	120	–	
Output Current – Scanner			4, 5				μA
V_{OH}=3.0 V	Source	I_{OH}	6, 7	4	−30	–	
V_{OL}=0.5 V	Sink	I_{OL}		4	245	–	
Output Current – Oscillator			13				μA
V_{OH}=3.0 V	Source	I_{OH}		4	−300	–	
V_{OL}=0.5 V	Sink	I_{OL}		4	245	–	
Input Current – Oscillator		I_{in}	12				μA
Operation				10	±2	±80	
Idle, V_{IL}=0.5 V				4	30	–	
Input Current – Decoder		I_{in}	1, 2, 3, 10				μA
V_{IH}=9 V			11, 14, 15	10	−15	–	
V_{IL}=0.5 V			16, 17	4	–	−60	
Input Voltage – Decoder			1, 2, 3, 10				V
		V_{IH}	11, 14, 15	10	9	–	
		V_{IL}	16, 17	10	–	1.2	
		V_{IH}		4	3	–	
		V_{IL}		4	–	1.0	

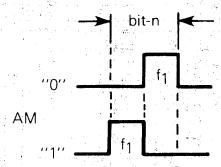
7

CIRCUIT OPERATION

The transmitter sends a 6-bit, labelled A (LSB) to F (MSB), binary code giving a total of 64 possible combinations or code words. All of these channels are user selectable, except the last two - where channel 63 is not sent while channel 62 is automatically sent by the transmitter at the end of each transmission as an "End of Transmission" code.

In either mode, FSK or AM, the transmitted signal is in the form of a biphase pulse code modulation (PCM) signal. The AM coding is shown in Figure 2.

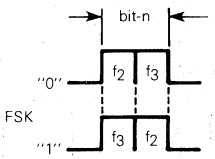
FIGURE 2 — AM CODING



In the AM mode, f_1 is a train of pulses at the modulating frequency of 31.25 kHz for a reference frequency of 500 kHz.

In the FSK mode, two modulating frequencies are used as shown in Figure 3.

FIGURE 3 — FSK CODING



In this mode, f_3 is 50 kHz and f_2 is 41.66 kHz for a reference frequency of 500 kHz.

The keyboard can be a simple switch matrix using no external diodes, connected to the four scanner outputs, A1 to A4, and the eight row inputs, E1 to E8. Under these conditions, only the first 32 code words are available since bit-F is always at logical "0". However, a simple two-pole changeover switch, in the manner of a typewriter "shift" key (switch FK3 in figure 1) can be used to change the polarity of bit-F to give access to the next full set of 32 instructions.

An alternative method of accessing more than 32 instructions is by the use of external diodes between the address inputs (see Figure 4). These have the effect of producing "phantom" address inputs by pulling two inputs low at the same time, which causes bit-F to go high, that is to logical "1". By interconnecting only certain address inputs it is possible to make an intermediate keyboard with between 32 and 64 keys.

The other two switches in Figure 1, FK1 and FK2, change the modulation mode. Closing FK1 changes the modulation from FSK to AM and the start-bit polarity. Closing FK2 changes the start-bit to a logical "0".

The full range of options available is illustrated in the table below:

	Start-bit	Modulation	Bit-F	Channels
E9 = Open	1	FSK	0	0-31
E9 = A1 (FK1)	1	AM	0	0-31
E9 = A2 (FK2)	0	FSK	0	0-31*
E9 = A3 (FK3)	1	FSK	1	32-61
E9 = A1•A2	0	AM	0	0-31
E9 = A1•A3	1	AM	1	32-61
E9 = A2•A3	0	FSK	1	32-61*
E9 = A1•A2•A3	0	AM	1	32-61

* Not allowed.

One of the transmitter's major features is its low power consumption - in the order of 10 μA in the idle state. For this reason the battery is perpetually in circuit. It has in fact been found that a light discharge current is beneficial to battery life.

In its active state, the transmitter efficiency is increased by the use of a low duty cycle which is less than 2.5% for the modulating pulse trains.

While no key is pressed, the circuit is in its idle state and the reference oscillator is stopped. Also, the eight address input lines are held high through internal pull-up resistors.

As soon as a key is pressed, this takes the appropriate address line low, signalling to the circuit that a key has been selected. The oscillator is now enabled. If the key is released before the code word has been sent, the circuit returns to its idle state. To account for accidental activation of the transmitter, the circuit has a built-in reaction time of ~20 ms, which also overcomes contact bounce. After this delay the code word will be sent and repeated at 90 ms intervals for as long as the key is pressed. As soon as the key is released, the circuit automatically sends channel 62, the "End of Transmission" (EOT) code. The transmitter then returns to its idle state.

The differences between the two modulation modes are illustrated in figure 5. However, it should be noted that in the AM mode, each transmitted word is preceded by a burst of pulses lasting 512 μs. This is used to set up the AGC loop in the receiver's preamp. In the FSK mode, the first frequency of the first bit is extended by 1.5 ms and the AGC burst is suppressed. In either mode it is assumed that the normal start-bit is present.

PIN DESCRIPTIONS

E1 to E8, ROW INPUTS (PINS 1, 2, 10, 11, 14, 15, 16, AND 17) — Under idle conditions, these inputs are held high by internal pull-up resistors. As soon as a key is pressed, a logical "0" on that particular line signals to the circuit that a key has been selected. After a delay of 20 ms, the internal register is loaded with the code word for the key selected.

E9, ROW INPUT (PIN 3) — This is a special programming input and when connected to the appropriate scanner output via a diode, it will modify the transmitted output according to the table in the Circuit Operation section.

In that table, the figures in brackets, FK1, etc., refer to the switches shown in Figures 1 and 4. If only one option is required, the diode may be omitted. The connections shown in the table may be made in any combination.

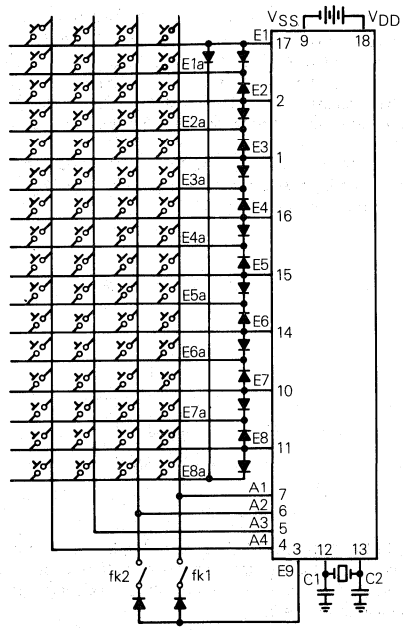
Although E9 is a row input, forcing this line low will not activate the circuit.

A1 to A4, SCANNER OUTPUTS (PINS 4, 5, 6 AND 7) — Under idle conditions, these outputs are held low, logical "0". When a key is pressed, the circuit is activated and the oscillator will start and release the outputs (see Figure 6).

Osc_{in}, Osc_{out}, OSCILLATOR INPUT AND OSCILLATOR OUTPUT (PINS 12 AND 13) — These are designed to operate with a 500 kHz ceramic resonator or a tuned LC circuit. It is important that a ceramic resonator and not a filter be used here, as the oscillator frequency cannot be guaranteed if a ceramic filter is used.

Signal Out, SIGNAL OUTPUT (PIN 8) — This output provides the modulating signal ready to drive the modulation amplifier. If required, the transmitter can be used as a keyboard encoder for direct use with a receiver. In this case, the AM option is selected, the output inverted and fed directly to the receiver's signal input pin.

FIGURE 4 — 64-KEY KEYBOARD



Note: Maximum key contact resistance = 1 kΩ.

7

FIGURE 5 — TRANSMITTED WAVEFORMS AND TIMING

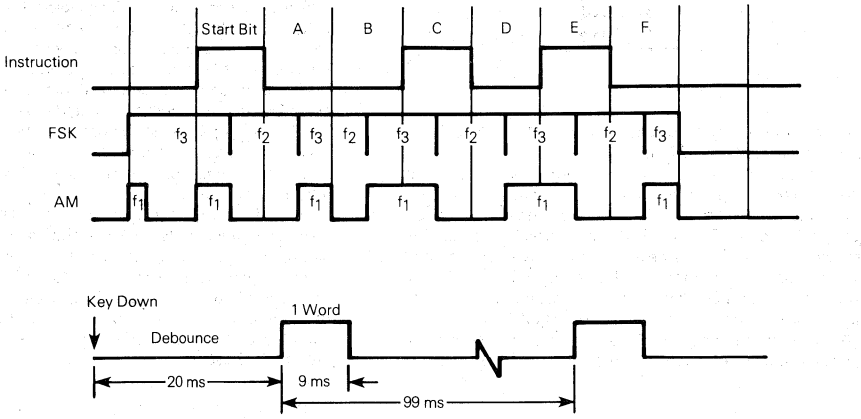


FIGURE 6 — SCANNER OUTPUT TIMING DIAGRAM

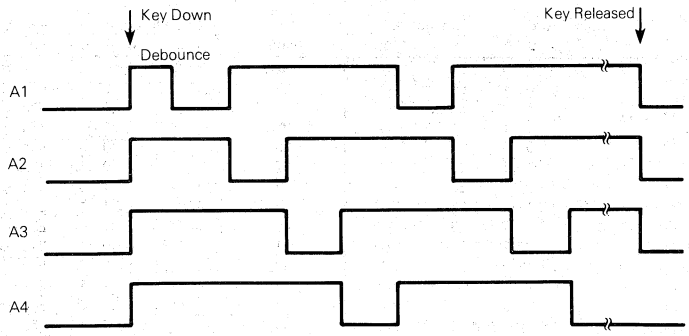


FIGURE 7 — TYPICAL APPLICATION CIRCUIT

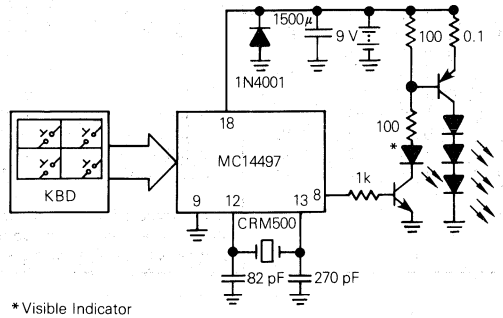


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TABLE 1 — TRANSMITTED CODES

Channel	Code Word F	E	D	C	B	A	Keyboard In	Out	Channel	Code Word F	E	D	C	B	A	Keyboard In	Out
0	0	0	0	0	0	0	E8	A4	32	1	0	0	0	0	0	E8a	A4
1				0	0	1	E1	A4	33				0	0	1	E1a	A4
2				0	1	0	E2	A4	34				0	1	0	E2a	A4
3				0	1	1	E3	A4	35				0	1	1	E3a	A4
4				1	0	0	E4	A4	36				1	0	0	E4a	A4
5				1	0	1	E5	A4	37				1	0	1	E5a	A4
6				1	1	0	E6	A4	38				1	1	0	E6a	A4
7				1	1	1	E7	A4	39				1	1	1	E7a	A4
8	0	0	1	0	0	0	E8	A1	40	1	0	1	0	0	0	E8a	A1
9				0	0	1	E1	A1	41				0	0	1	E1a	A1
10				0	1	0	E2	A1	42				0	1	0	E2a	A1
11				0	1	1	E3	A1	43				0	1	1	E3a	A1
12				1	0	0	E4	A1	44				1	0	0	E4a	A1
13				1	0	1	E5	A1	45				1	0	1	E5a	A1
14				1	1	0	E6	A1	46				1	1	0	E6a	A1
15				1	1	1	E7	A1	47				1	1	1	E7a	A1
16	0	1	0	0	0	0	E8	A3	48	1	1	0	0	0	0	E8a	A3
17				0	0	1	E1	A3	49				0	0	1	E1a	A3
18				0	1	0	E2	A3	50				0	1	0	E2a	A3
19				0	1	1	E3	A3	51				0	1	1	E3a	A3
20				1	0	0	E4	A3	52				1	0	0	E4a	A3
21				1	0	1	E5	A3	53				1	0	1	E5a	A3
22				1	1	0	E6	A3	54				1	1	0	E6a	A3
23				1	1	1	E7	A3	55				1	1	1	E7a	A3
24	0	1	1	0	0	0	E8	A2	56	1	1	1	0	0	0	E8a	A2
25				0	0	1	E1	A2	57				0	0	1	E1a	A2
26				0	1	0	E2	A2	58				0	1	0	E2a	A2
27				0	1	1	E3	A2	59				0	1	1	E3a	A2
28				1	0	0	E4	A2	60				1	0	0	E4a	A2
29				1	0	1	E5	A2	61				1	0	1	E5a	A2
30				1	1	0	E6	A2	62 (EOT)				1	1	0	E6a	A2
31	0	1	1	1	1	1	E7	A2	Not transmitted	1	1	1	1	1	1	E7a	A2

NOTE: Although the "a" suffix applies to a phantom input when using a keyboard with up to 64 keys, the coding is identical with a 32 key keyboard when switch FK3 is closed.

7

MOTOROLA

MC145026
MC145027
MC145028
MC145029

Advance Information

MC145026 ENCODER, MC145027/MC145028/MC145029 DECODERS

The MC145026 will encode nine bits of information and serially transmit this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0, 1, open) allowing 3^9 (19,683) different codes.

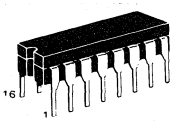
Three decoders are presently available; all use the same transmitter – the MC145026. The decoders receive the 9-bit word and interpret some of the bits as address codes and some as data. The MC145027 interprets the first five transmitted bits as address and the last four bits as data. The MC145029 interprets the first four transmitted bits as address and the last five bits as data. The MC145028 treats all nine bits as address. If no errors are received, the MC145027 outputs four data bits, and the MC145029 outputs five data bits, when the transmitter sends address codes that match that of the receiver. A valid transmission output will go high on the decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

- May be Addressed in either Binary or Trinary
- Trinary Addressing Maximizes Number of Codes
- Interfaces with RF, Ultrasonic, or Infrared Transmission Medias
- On-Chip R/C Oscillator; No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Standard B-Series Input and Output Characteristics
- 4.5 to 18 V Operation
- 2.9 V Low-Voltage Version Also Available by Special Order

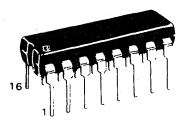
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

REMOTE CONTROL ENCODER/DECODER PAIRS



L SUFFIX
CERAMIC PACKAGE
CASE 620

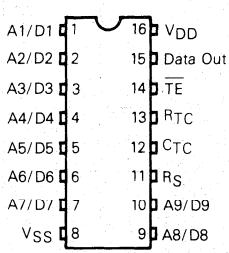


P SUFFIX
PLASTIC PACKAGE
CASE 648

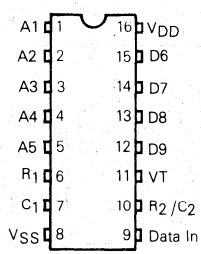
MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

7

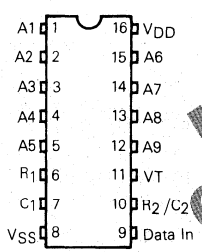
PIN ASSIGNMENTS



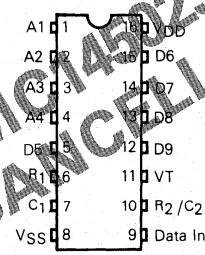
MC145026
Encoder



MC145027
Decoder



MC145028
Decoder



MC145029
Decoder

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level		5.0	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{DD} or 0	V_{OL}	10	–	0.05	–	0	0.05	–	0.05	V
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	
V_{in} = 0 or V_{DD}	V_{OH}	10	9.95	–	9.95	10	–	9.95	–	V
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level										
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)	V_{IL}	10	–	3.0	–	4.50	3.0	–	3.0	V
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.25	4.0	–	4.0	
"1" Level										
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)	V_{IH}	10	7.0	–	7.0	5.50	–	7.0	–	V
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current Source										
(V_{OH} = 2.5 V)		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V)	I_{OH}	5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	mA
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 V) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)	I_{OL}	10	1.3	–	1.1	2.25	–	0.9	–	mA
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current – $\overline{TE}$ (MC145026, Pullup Device)		5.0	–	–	3.0	4.0	9.0	–	–	
	I_{in}	10	–	–	16	20	32	–	–	μA
		15	–	–	35	45	70	–	–	
Input Current										
R_S (MC145026)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Data In (MC145027, MC145028, MC145029)										
Input Current										
A1/D1-A9/D9 (MC145026)		5.0	–	–	–	±55	±110	–	–	
A1-A5 (MC145027)	I_{in}	10	–	–	–	±300	±500	–	–	μA
A1-A9 (MC145028)		15	–	–	–	±650	±1000	–	–	
A1-A4 (MC145029)										
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current – MC145026		5.0	–	–	–	0.0050	0.10	–	–	
	I_{DD}	10	–	–	–	0.0100	0.20	–	–	μA
		15	–	–	–	0.0150	0.30	–	–	
Quiescent Current – MC145027, MC145028, MC145029		5.0	–	–	–	30	50	–	–	
	I_{DD}	10	–	–	–	60	100	–	–	μA
		15	–	–	–	90	150	–	–	
Total Supply Current – MC145026 (f_c = 20 kHz)		5.0	–	–	–	100	200	–	–	
	I_T	10	–	–	–	200	400	–	–	μA
		15	–	–	–	300	600	–	–	
Total Supply Current – MC145027, MC145028, MC145029		5.0	–	–	–	200	400	–	–	
(f_c = 20 kHz)	I_T	10	–	–	–	400	800	–	–	μA
		15	–	–	–	600	1200	–	–	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}	5.0	–	100	200	ns
	t_{THL}	10	–	50	100	
		15	–	40	80	
Data In Rise and Fall Time (MC145027, MC145028, MC145029)	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	15	
		15	–	–	15	
Encoder Clock Frequency	f_{cl}	5.0	0	–	2	MHz
		10	0	–	5	
		15	0	–	10	
Decoder Frequency (Referenced to Encoder Clock) (See Figure 10)	f_{cl}	5.0	1	–	240	kHz
		10	1	–	410	
		15	1	–	450	
$\overline{TE}$ Pulse Width	t_{WL}	5.0	65	–	–	ns
		10	30	–	–	
		15	20	–	–	
System Propagation Delay ($\overline{TE}$ to Valid Transmission)	–	–	–	182	–	Clock Cycles
Tolerance on Timing Components ($\Delta R_{TC} + \Delta C_{TC} + \Delta R_1 + \Delta C_1$)	–	–	–	–	±25	%
($\Delta R_2 + \Delta C_2$)		–	–	–	±25	

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins may be in either of three states (0, 1, open) allowing $3^9 = 19{,}683$ possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder outputs two identical data words. Between the two data words no signal is sent for three data bit times. If the $\overline{TE}$ input is kept low, the encoder continuously transmits the data word.

Each transmitted data bit is encoded into two data pulses (See Figure 7). A logic zero is encoded as two consecutive short pulses, a logic one as two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The $\overline{TE}$ input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the Data Out output pin.

Transmission must be initiated by using the $\overline{TE}$ pin rather than by holding $\overline{TE}$ low and applying power to the device because an internal reset occurs after the first transmit sequence.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical data words, is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address input at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches by VT and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid address has been received.

Although address information is normally encoded in trinary, the designer should be aware that, for the MC145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only $2 \times 3^8 = 13{,}122$ different codes. A trinary (open) A9 will be interpreted as a logic 1. However, if the encoder sends a trinary (or logic 1) and the decoder address is a logic 1 (or trinary) respectively, the valid transmission output length will be shortened to the $R1 \times C1$ time constant.

MC145029

This decoder operates like the MC145027, but it assumes the first four received bits to be address bits and the remaining five received bits to be data.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words for error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a vaild transmission output.

PIN DESCRIPTIONS

MC145026 ENCODER

A1/D1-A9/D9, ADDRESS/DATA INPUTS (PINS 1, 2, 3, 4, 5, 6, 7, 9, 10) — These inputs are encoded and the data is serially output from the encoder.

R_S, C_{TC}, R_{TC}, OSCILLATOR COMPONENTS (PINS 11, 12, 13) — These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$, TRANSMIT-ENABLE INPUT (PIN 14) This active low input initiates transmission when forced low. An internal pullup device keeps this input normally high.

Data Out, DATA OUTPUT (PIN 15) — This is the output of the encoder that serially presents the encoded word.

V_{DD}, POSITIVE SUPPLY (PIN 16) — The most positive power supply.

V_{SS}, NEGATIVE SUPPLY (PIN 8) — The most negative supply (usually ground).

MC145027, MC145028, MC145029 DECODERS

A1-A5 (MC145027), A1-A9 (MC145028), A1-A4 (MC145029), ADDRESS INPUTS — These address inputs must match the corresponding encoder inputs in order for the decoder to output data.

D6-D9 (MC145027), D5-D9 (MC145029), DATA OUTPUTS — These outputs present the information that is on the corresponding encoder inputs. Note: only binary data will be acknowledged; a trinary open will be decoded as a logic one.

R_1, C_1, PULSE DISCRIMINATOR (PINS 6, 7) — These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant $R_1 \times C_1$ should be set to 1.72 encoder (transmitter) clock periods. $R_1C_1 = 3.95\ R_{TC}C_{TC}$.

R_2/C_2, DEAD TIME DISCRIMINATOR (PIN 10) — This pin accepts a resistor and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder (transmitter) clock periods (four data bit periods): $R_2C_2 = 77\ R_{TC}C_{TC}$. This time constant is used to determine that Data In has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage-equivalent two data bit times ($0.4\ R_2C_2$) to detect the dead time between transmitted words.

VT, VALID TRANSMISSION (PIN 11) — This output goes high when the following conditions are satisfied:

1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (MC145027 and MC145029, only).

VT will remain high until a mismatch is received, or no input signal is received for four data bit times.

V_{DD}, POSITIVE SUPPLY (PIN 16) — The most positive power supply.

V_{SS}, NEGATIVE SUPPLY (PIN 8) — The most negative supply (usually ground).

FIGURE 1— MC145026 ENCODER BLOCK DIAGRAM

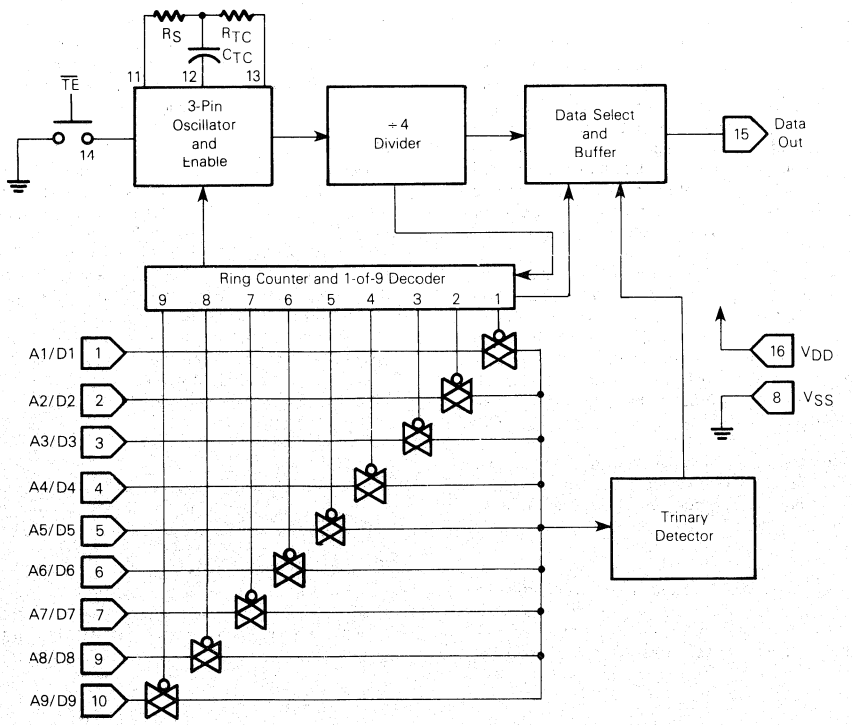


FIGURE 2 — MC145027 DECODER BLOCK DIAGRAM

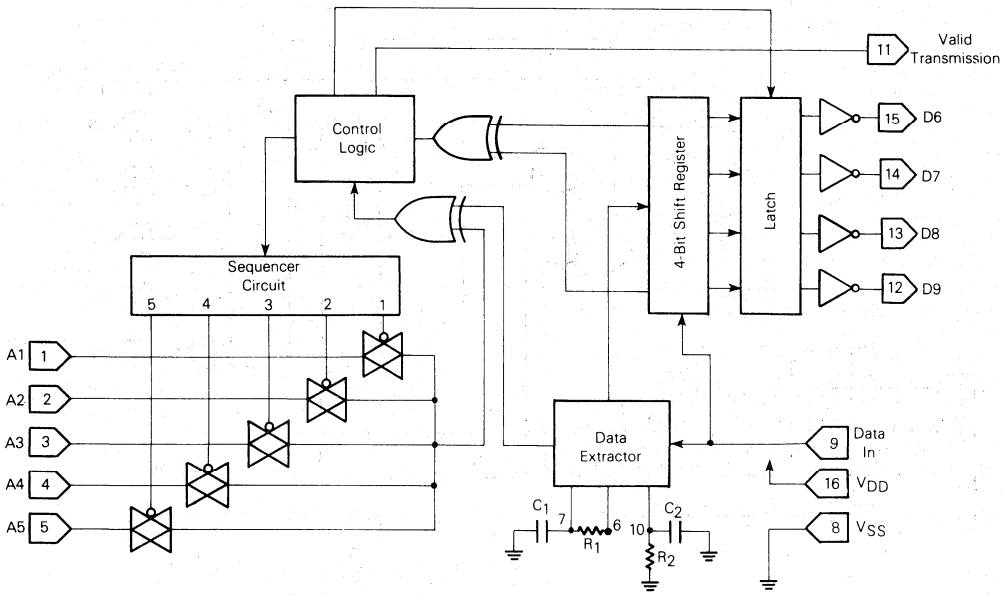


FIGURE 3 — MC145028 DECODER BLOCK DIAGRAM

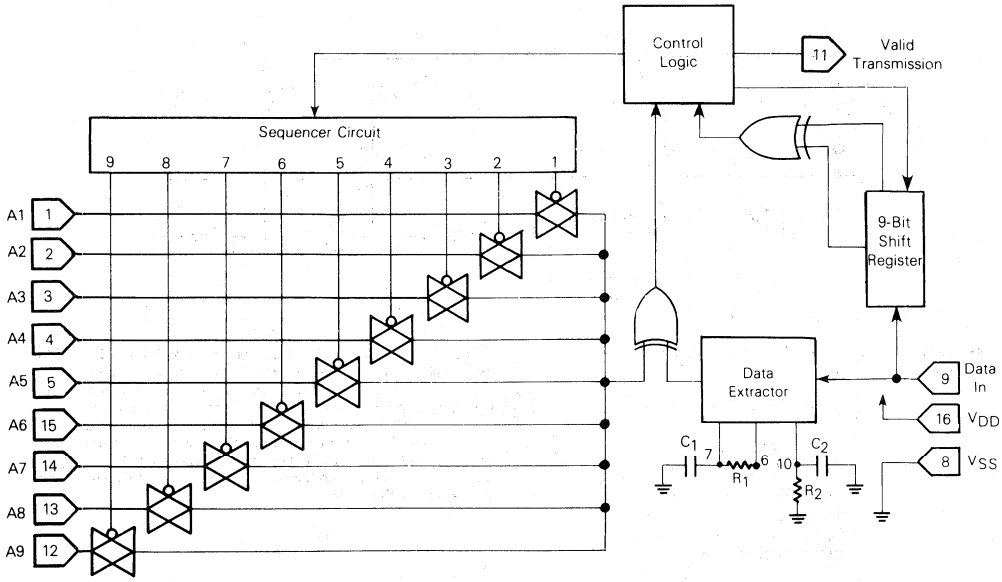


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FIGURE 4 — MC145029 DECODER BLOCK DIAGRAM

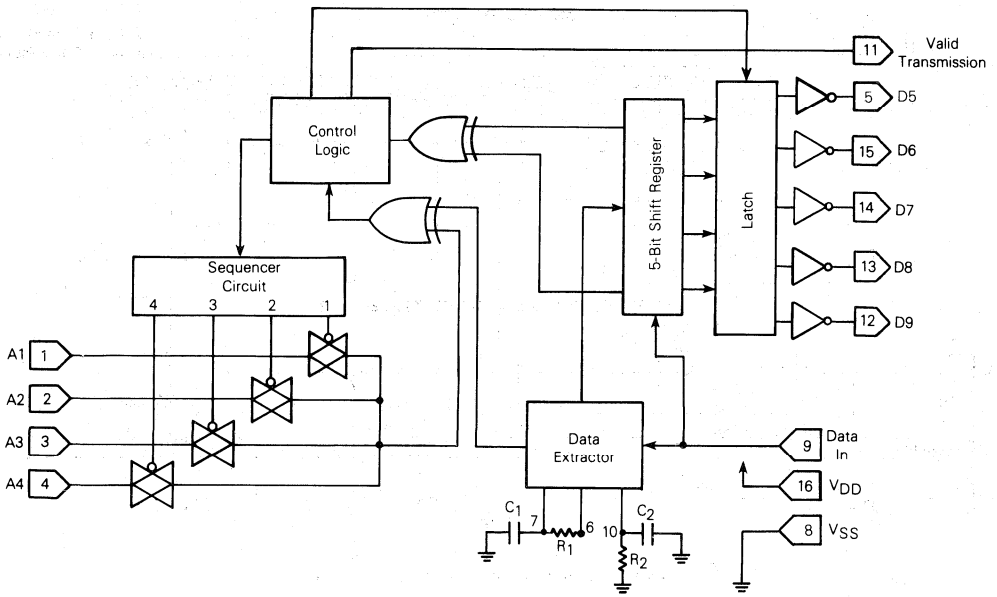
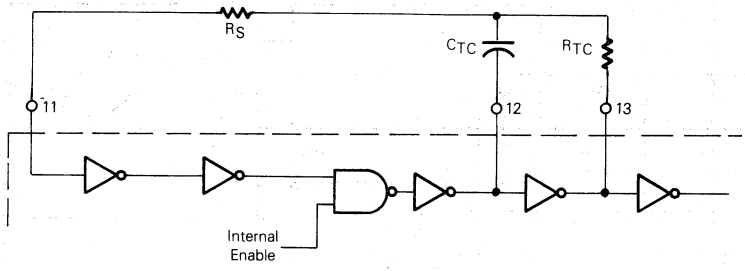


FIGURE 5 — ENCODER OSCILLATOR INFORMATION



This oscillator will operate at a frequency determined by the external RC network; i.e.,

$$f \cong \frac{1}{2.3\ R_{TC}\ C_{TC}'}\ (Hz)$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < C_{TC} < 15 μF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range will ensure that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that $R_S \times 5$ pF (input capacitance) is small compared to $R_{TC} \times C_{TC}$.

For frequencies outside the indicated range, the formula will be less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

FIGURE 6 – ENCODER/DECODER TIMING DIAGRAM

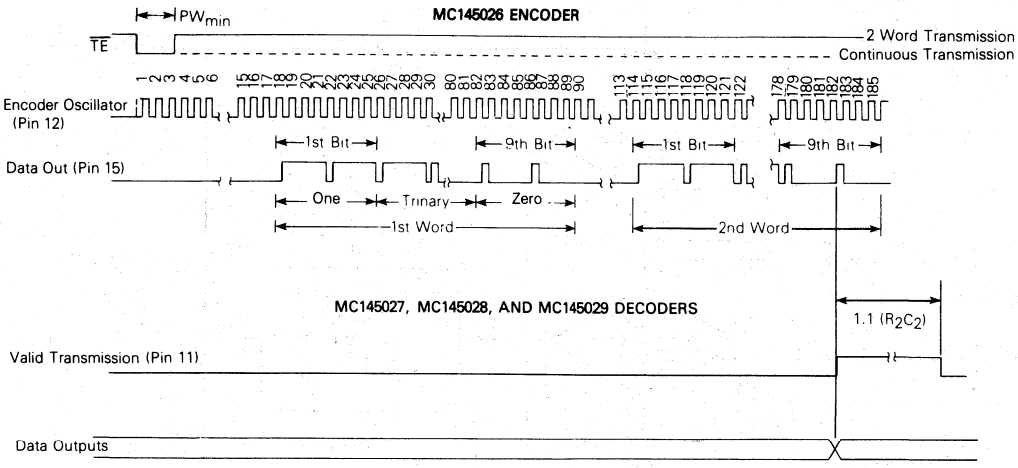


FIGURE 7 – MC145026 ENCODER DATA WAVEFORMS

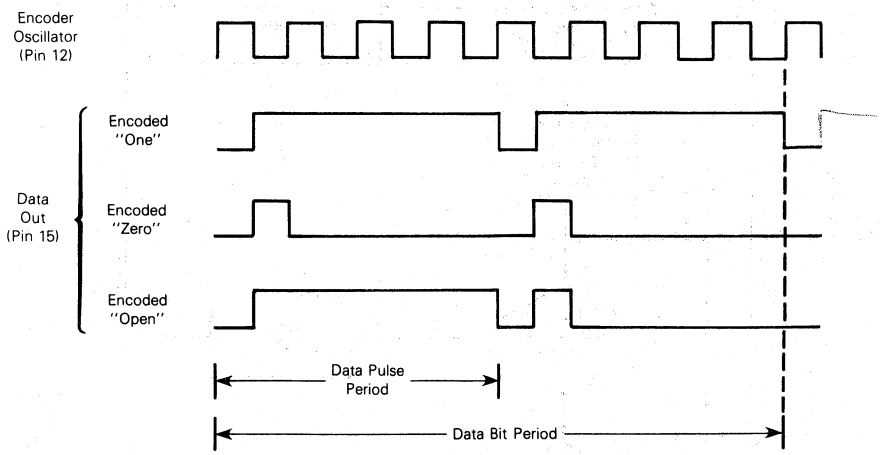


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FIGURE 8 — MC145027/MC145029 FLOWCHART

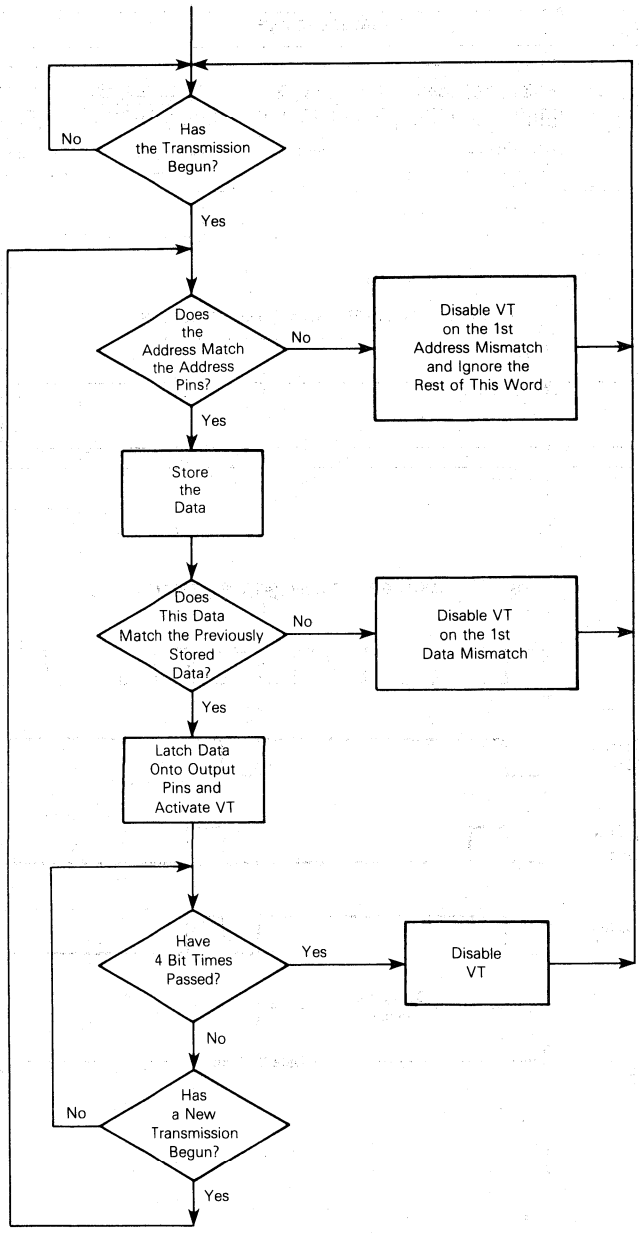
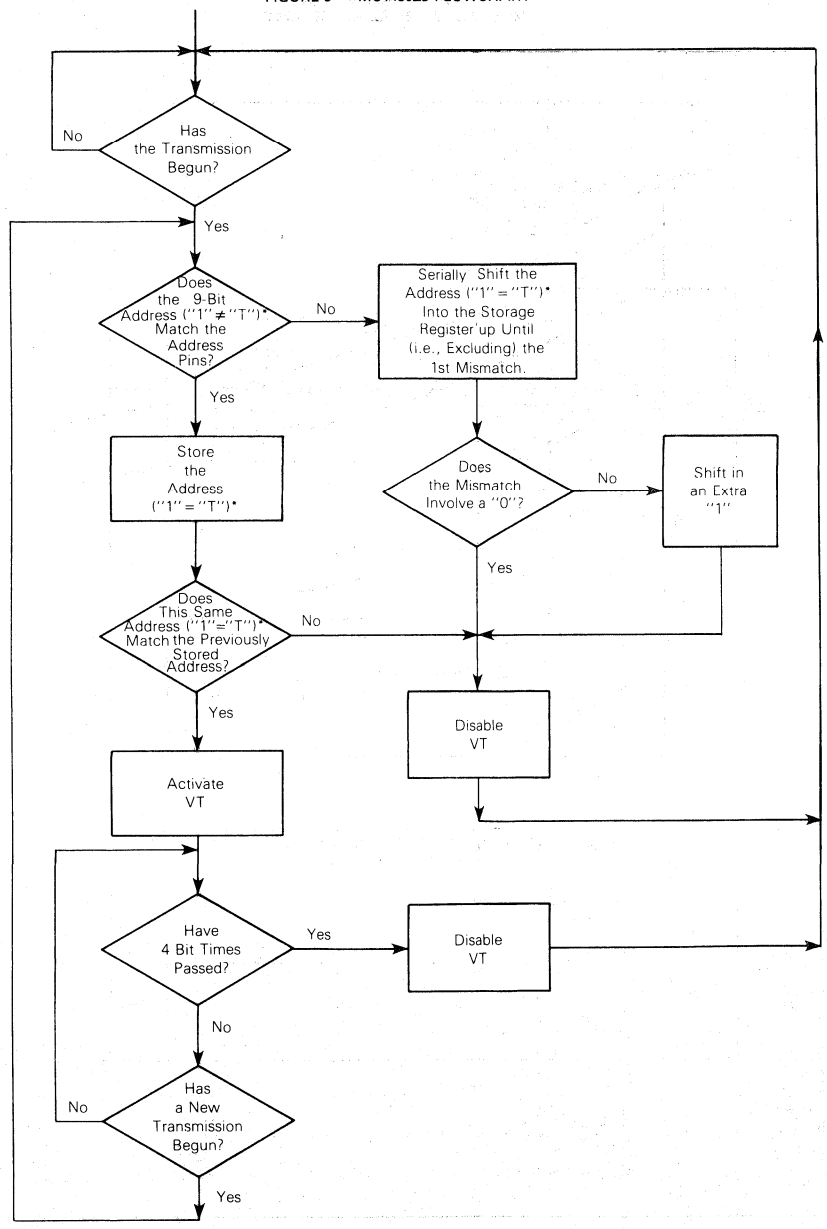
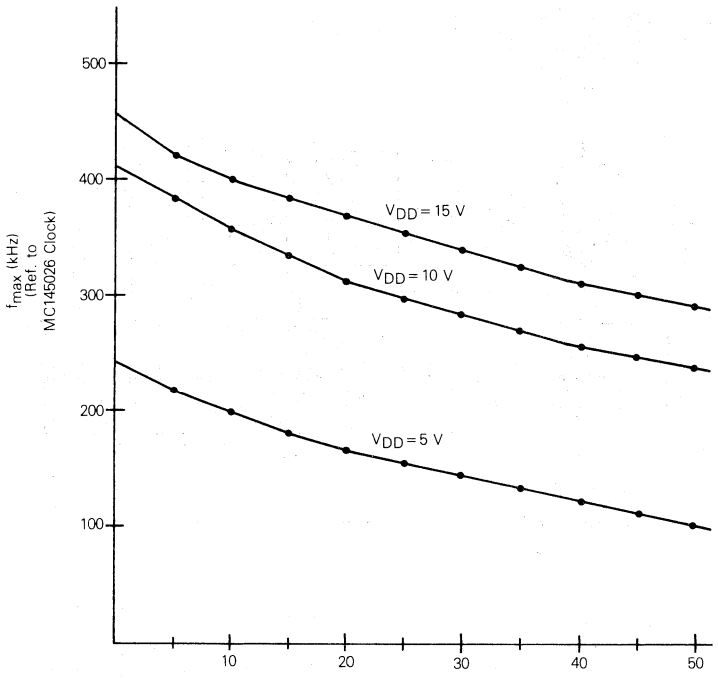


FIGURE 9 — MC145028 FLOWCHART



*For shift register comparisons, a "T" is stored as a "1".

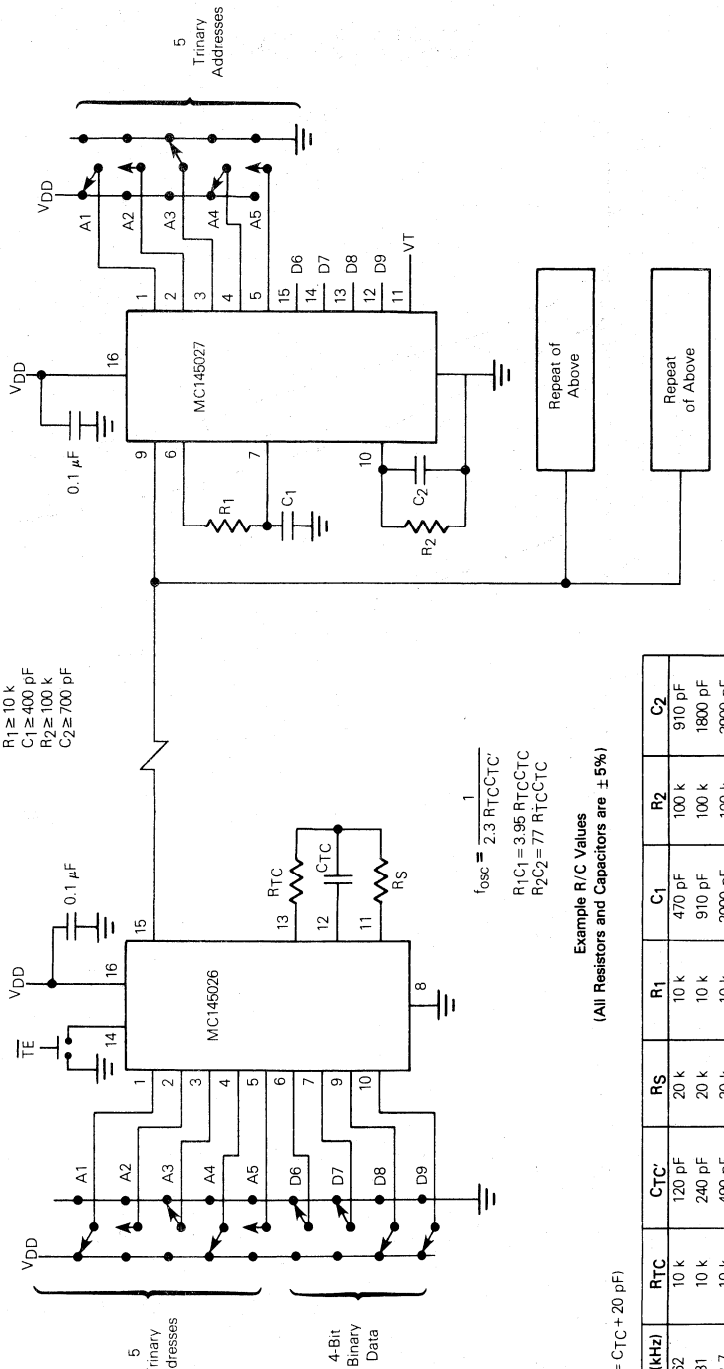
FIGURE 10 — f_{max} vs C_{layout}
MC145027, MC145028, and MC145029



C_{layout} (pF) on Pins 1-5 (MC145027); Pins 1-5 and 12-15 (MC145028);
Pins 1-4 (MC145029)

7

FIGURE 11 – TYPICAL APPLICATION



$C_{TC'} = C_{TC} + C_{layout} + 12$ pF
100 pF ≤ C_{TC} ≤ 15 µF
R_{TC} ≥ 10 k; $R_S \approx 2\,R_{TC}$
R_1 ≥ 10 k
C_1 ≥ 400 pF
R_2 ≥ 100 k
C_2 ≥ 700 pF

$$f_{osc} = \frac{1}{2.3\,R_{TC}C_{TC'}}$$

$R_1C_1 = 3.95\,R_{TC}C_{TC}$
$R_2C_2 = 77\,R_{TC}C_{TC}$

Example R/C Values
(All Resistors and Capacitors are ±5%)

($C_{TC'} = C_{TC} + 20$ pF)

f_{osc} (kHz)	R_{TC}	$C_{TC'}$	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

CMOS Smoke Detectors

8

CMOS SMOKE DETECTORS

Device Number	Function
MC14466	Low Cost Smoke Detector
MC14467-1	Low Cost Smoke Detector
MC14468	Interconnectable Smoke Detector

Function	On-Chip High Input Impedance FET Comparator	Low Battery Detector	Piezoelectric Horn Driver	Device Number	Number of Pins
Ionization-Type Smoke Detector	✓	✓	✓	MC14466	16
	✓	✓	✓	MC14467-1	16
Ionization-Type Smoke Detector with Interconnect	✓	✓	✓	MC14468	16

MOTOROLA

MC14466

LOW-COST SMOKE DETECTOR

The MC14466, together with an ionization chamber, will detect smoke using a minimum of external components. When smoke is sensed, an alarm is sounded via an external piezoelectric transducer and internal drivers. This circuit is designed to comply with the UL217 specification.

- Ionization Type with On-Chip FET Input Comparator
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Low Battery Trip Point Internally Set Can Be Altered Via External Resistor
- Detect Threshold Internally Set Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Outputs for Detect and Low Battery
- Internal Reverse Battery Protection
- Chip Complexity: 239 FETs

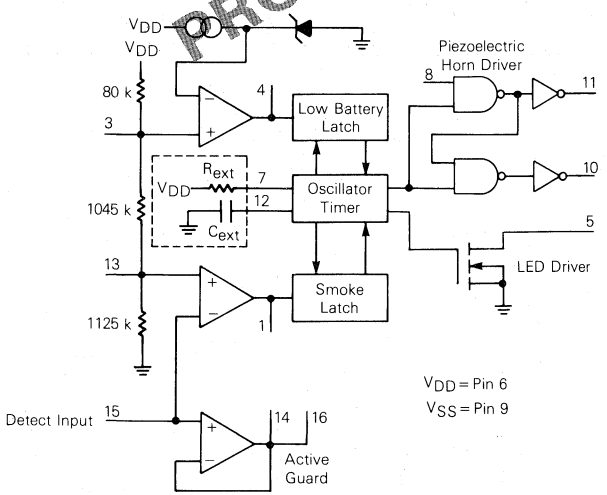
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

LOW-COST SMOKE DETECTOR

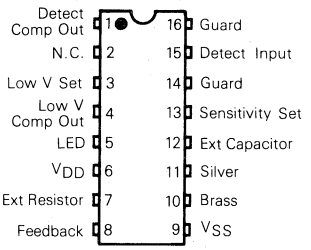
P SUFFIX
PLASTIC PACKAGE
CASE 648B*

*Pins 15 and 16 are connected via a metal shorting bar. See package detail in Figure 1.

BLOCK DIAGRAM



PIN ASSIGNMENT



8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs	V_{in}	−0.25 to V_{DD}+0.25	V
DC Input Current, per Pin	I_{in}	10	mA
DC Output Current, per Pin	I_{out}	30	mA
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Reverse Battery Time	t_{RB}	5.0	s

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

RECOMMENDED DC OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	9.0	V
Timing Capacitor	C_{ext}	0.1	μF
Timing Resistor	R_{ext}	8.2	MΩ
Battery Load (Resistor or LED)	–	10	mA

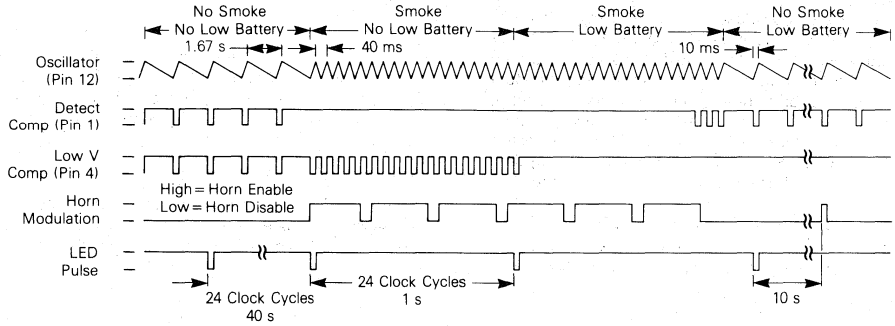
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	–	6.0	–	10	V
Output Voltage	V_{OH}					V
Piezoelectric Horn Drivers (I_{OH} = 16 mA)		7.4	6.5	–	–	
Comparators (I_{OH} = 30 μA)		9.0	8.5	8.8	–	
Piezoelectric Horn Drivers (I_{OL} = −16 mA)	V_{OL}	7.4	–	–	0.9	
Comparators (I_{OL} = −30 μA)		9.0	–	0.1	0.5	
Output Current – LED Driver (V_{OL} = 3.0 V)	I_{OL}	7.4	10	–	–	mA
Operating Current (R_{ext} = 8.2 MΩ)	I_{DD}	9.0	–	5.0	9.0	μA
Input Current – Detect (40% R.H.)	I_{in}	9.0	–	–	±1.0	pA
Internal Set Voltage – Low Battery	V_{low}	9.0	7.2	–	7.8	V
– Sensitivity	V_{set}	–	47	50	53	%V_{DD}
Hysteresis	V_{hys}	9.0	75	100	150	mV
Offset Voltage (measured at $V_{in} = V_{DD}/2$)	V_{OS}					mV
Active Guard		9.0	–	–	±100	
Detect Comparator		9.0	–	–	±50	

TIMING PARAMETERS (C_{ext} = 0.1 μF, R_{ext} = 8.2 MΩ, V_{DD} = 9.0 V, T_A = 25°C)

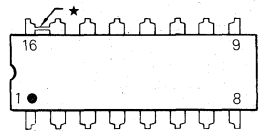
Characteristics		Min	Typ	Max	Units
Oscillator Period	No Smoke	1.34	1.67	2.0	s
	Smoke	32	40	48	ms
Oscillator Rise Time (Pin 12)		8	10	12	ms
Horn Output	On Time	120	160	208	ms
(During Smoke)	Off Time	60	80	104	ms
LED Output	Off Time Between Pulses	32	40	48	s
(During No Smoke)	On Time	8	10	12	ms
Horn Output	On Time	8	10	12	ms
(During Low Battery)	Off Time Between Pulses	32	40	48	s

TIMING DIAGRAM



NOTES: 1. Horn modulation is self-completing. When going from smoke to no smoke, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no smoke, 40 μ s for smoke).
3. Low battery comparator information is latched only during LED pulse.

FIGURE 1 — PACKAGE DETAIL



★ External lead connection (shorting bar) between Pins 15 and 16.

8

DEVICE OPERATION

TIMING

The internal oscillator of the MC14466 operates with a period of 1.67 seconds during no-smoke conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for smoke. Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage. Since very small currents are used in the oscillator, the oscillator capacitor should be of a low leakage type.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 200 ms on, 40 ms off. During the off time, smoke is again checked and will inhibit further horn output if no smoke is sensed. During smoke conditions the low battery detection is inhibited, but the LED pulses at a 1.0 Hz rate.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins will be within 100 mV of the input signal. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard op amp is not power strobed and thus gives constant protection from surface leakage current. Pin 16 of the active guard is connected to Pin 15 (the detect input) during shipping to protect Pin 15 from static damage (see Figure 1).

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider connected between V_{DD} and V_{SS}. These voltages can be altered by external resistors connected from Pins 3 or 13 to either V_{DD} or V_{SS}. There will be a slight interaction here due to the common voltage divider network.

TEST MODE

Since the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level could be difficult and/or time-consuming. By forcing Pin 12 to V_{SS}, the power strobing is bypassed and the outputs, Pins 1 and 4, constantly show smoke/no-smoke and good battery/low battery, respectively. Pin 1 = V_{DD} for smoke and Pin 4 = V_{DD} for low battery. In this mode and during the 10ms power strobe, chip current rises to approximately 50 μA.

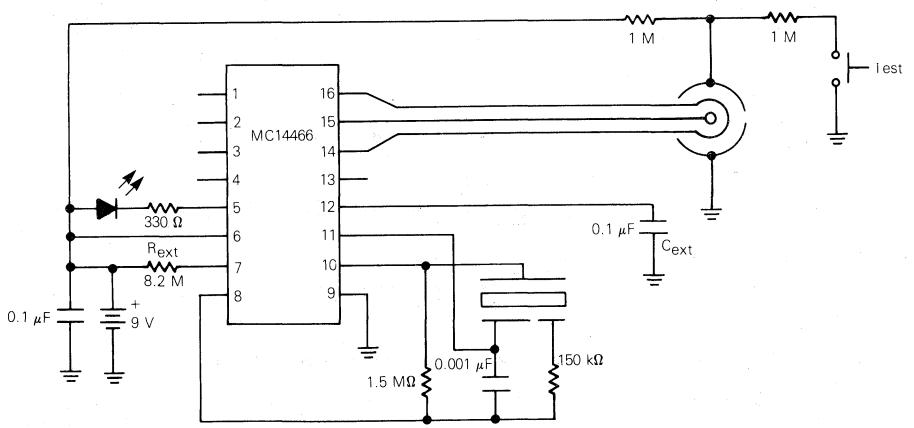
LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

HYSTERESIS

When smoke is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and avoids false triggering.

FIGURE 2 — TYPICAL APPLICATION AS IONIZATION SMOKE DETECTOR



NOTE: Component values may change depending on type of piezoelectric horn used.

FIGURE 3 — TYPICAL LED OUTPUT
I-V CHARACTERISTIC

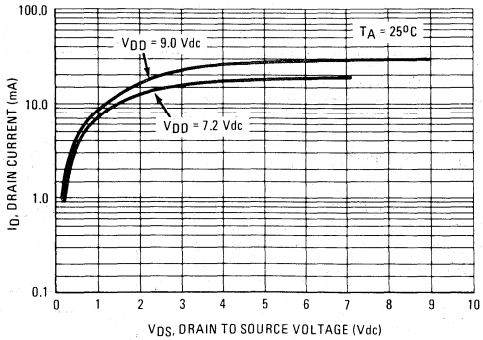
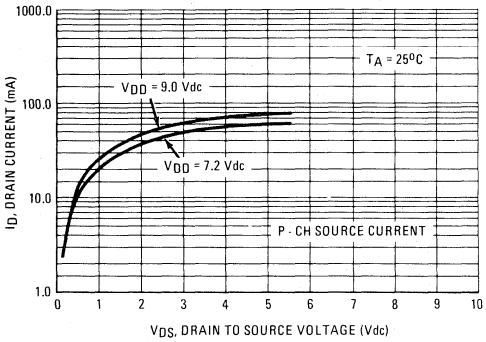


FIGURE 4 — TYPICAL P HORN DRIVER OUTPUT
I-V CHARACTERISTIC



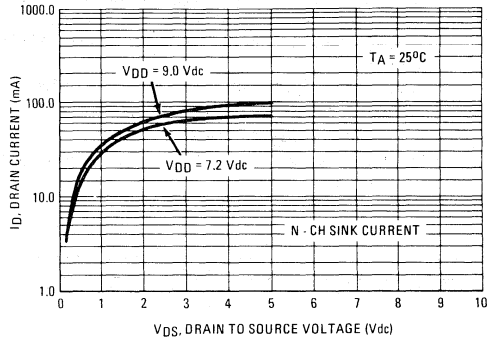
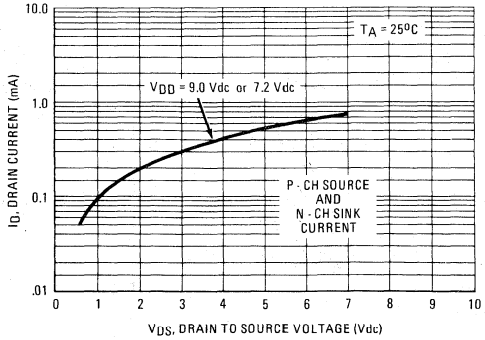


FIGURE 5 — TYPICAL COMPARATOR OUTPUT
I-V CHARACTERISTIC



8

MOTOROLA

MC14467-1

Advance Information

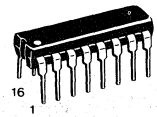
LOW-COST SMOKE DETECTOR

The MC14467-1, when used with an ionization chamber and a small number of external components, will detect smoke. When smoke is sensed, an alarm is sounded via an external piezoelectric transducer and internal drivers. This circuit is designed to comply with the UL217 specification.

- Ionization Type with On-Chip FET Input Comparator
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Input-Protection Diodes on the Detect Input
- Low-Battery Trip Point, Internally Set, Can Be Altered Via External Resistor
- Detect Threshold, Internally Set, Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Outputs for Detect and Low Battery
- Internal Reverse Battery Protection
- Direct Replacement for the MC14467, with Improved Alarm Stability

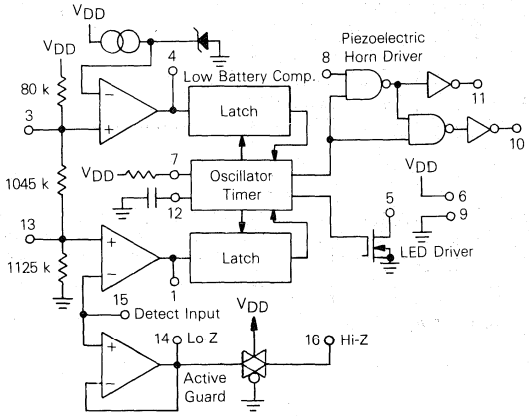
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

LOW-COST SMOKE DETECTOR

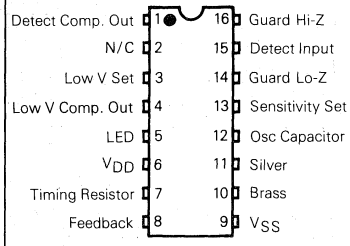


MC14467P1
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs Except Pin 8	V_{in}	−0.25 to V_{DD} +0.25	V
DC Current Drain per Input Pin, Except Pin 15 = 1 mA	I	10	mA
DC Current Drain per Output Pin	I	30	mA
Operating Temperature Range	T_A	−10 to +60	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Reverse Battery Time	t_{RB}	5.0	s

*Maximum Ratings are those values beyond which damage to the device may occur.

RECOMMENDED DC OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	9.0	V
Timing Capacitor	–	0.1	μF
Timing Resistor	–	8.2	MΩ
Battery Load (Resistor or LED)	–	10	mA

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS}, T_A = 25°C)

Characteristic		Symbol	V_{DD} V_{dc}	Min	Typ	Max	Unit
Operating Voltage		V_{DD}	–	6.0	–	12	V
Output Voltage		V_{OH}					V
Piezoelectric Horn Drivers (I_{OH} = −16 mA)			7.2	6.3	–	–	
Comparators (I_{OH} = −30 μA)			9.0	8.5	8.8	–	
Piezoelectric Horn Drivers (I_{OL} = +16 mA)		V_{OL}	7.2	–	–	0.9	V
Comparators (I_{OL} = +30 μA)			9.0	–	0.1	0.5	
Output Voltage — LED Driver, I_{OL} = 10 mA		V_{OL}	7.2	–	–	3.0	V
Output Impedance, Active Guard	Pin 14	Lo-Z	9.0	–	10	–	kΩ
	Pin 16	Hi-Z	9.0	–	500	–	
Operating Current (R_{bias} = 8.2 MΩ)		I_{DD}	9.0	–	5.0	9.0	μA
			12.0	–	–	12.0	
Input Current — Detect (40% R.H.)		I_{in}	9.0	–	–	±1.0	pA
Internal Set Voltage							
Low Battery		V_{low}	9.0	7.2	–	7.8	V
Sensitivity		V_{set}	–	47	50	53	%V_{DD}
Hysteresis		V_{hys}	9.0	75	100	150	mV
Offset Voltage (measured at V_{in} = V_{DD}/2)		V_{OS}					mV
Active Guard			9.0	–	–	±100	
Detect Comparator			9.0	–	–	±50	
Input Voltage Range, Pin 8		V_{in}	–	−10	–	V_{DD} + 10	V
Input Capacitance		C_{in}	–	–	5.0	–	pF
Common Mode Voltage Range, Pin 15		V_{cm}	–	0.6	–	V_{DD} − 2	V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that except for pin 8, V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. For pin 8, refer to the Electrical Characteristics.

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DEVICE OPERATION

TIMING

The internal oscillator of the MC14467-1 operates with a period of 1.67 seconds during no-smoke conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for smoke, except during LED pulse, Low Battery Alarm Chirp, or Horn Modulation (in smoke). Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage. Since very small currents are used in the oscillator, the oscillator capacitor should be of a low leakage type.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 160 ms on, 80 ms off. During the off time, smoke is again checked and will inhibit further horn output if no smoke is sensed. During smoke conditions the low battery alarm is inhibited, but the LED pulses at a 1.0 Hz rate.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins will be within 100 mV of the input signal. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. Pin 15 (the Detect input) has internal diode protection against static damage.

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider connected between V_{DD} and V_{SS}. These voltages can be altered by external resistors connected from pins 3 or 13 to either V_{DD} or V_{SS}. There will be a slight interaction here due to the common voltage divider network.

TEST MODE

Since the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level could be difficult and/or time-consuming. By forcing Pin 12 to V_{SS}, the power strobing is bypassed and the outputs, Pins 1 and 4, constantly show smoke/no smoke and good battery/low battery, respectively. Pin 1 = V_{DD} for smoke and Pin 4 = V_{DD} for low battery. In this mode and during the 10 ms power strobe, chip current rises to approximately 50 μA.

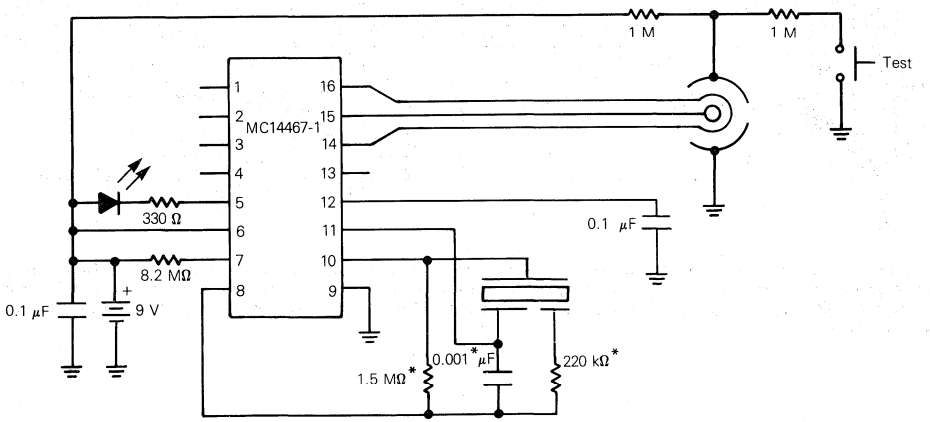
LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

HYSTERESIS

When smoke is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and reduces false triggering.

FIGURE 1 — TYPICAL APPLICATION AS IONIZATION SMOKE DETECTOR



*NOTE: Component values may change depending on type of piezoelectric horn used.

TIMING PARAMETERS ($C = 0.1\ \mu F$, $R_{bias} = 8.2\ M\Omega$, $V_{DD} = 9.0\ V$, $T_A = 25°C$, See Figure 5)

Characteristics		Symbol	Min	Typ	Max	Units
Oscillator Period	No Smoke	t_{Cl}	1.34	1.67	2.0	s
	Smoke		32	40	48	ms
Oscillator Rise Time		t_r	8	10	12	ms
Horn Output	On Time	PW_{on}	120	160	208	ms
(During Smoke)	Off Time	PW_{off}	60	80	104	ms
LED Output	Between Pulses	t_{LED}	32	40	48	s
	On Time	PW_{on}	8	10	12	ms
Horn Output	On Time	t_{on}	8	10	12	ms
(During Low Battery)	Between Pulses	t_{off}	32	40	48	s

FIGURE 2 — TYPICAL LED OUTPUT I-V CHARACTERISTIC

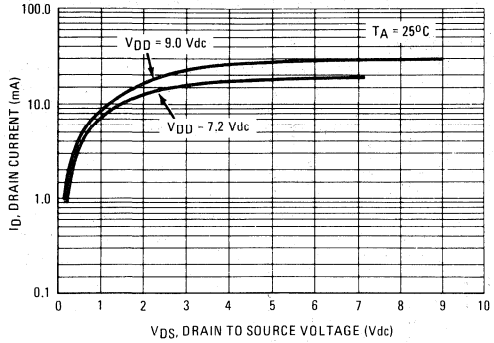


FIGURE 3 — TYPICAL COMPARATOR OUTPUT I-V CHARACTERISTIC

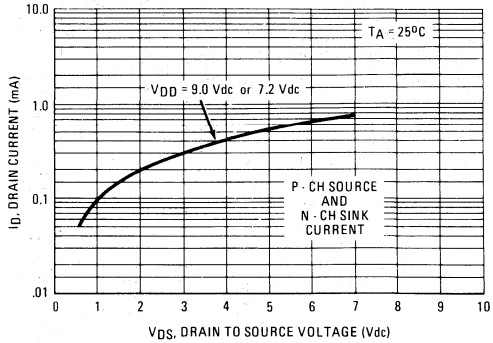
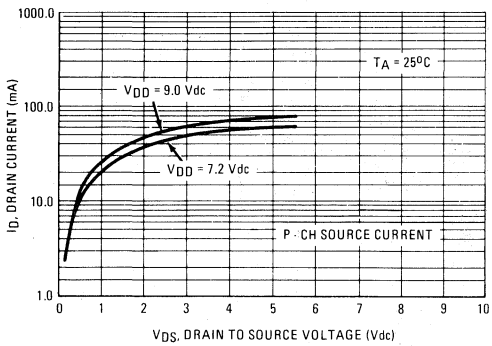


FIGURE 4 — TYPICAL P HORN DRIVER OUTPUT I-V CHARACTERISTIC



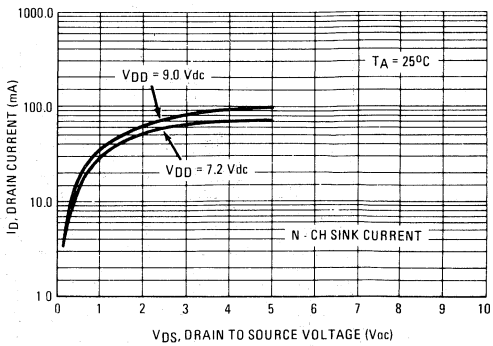


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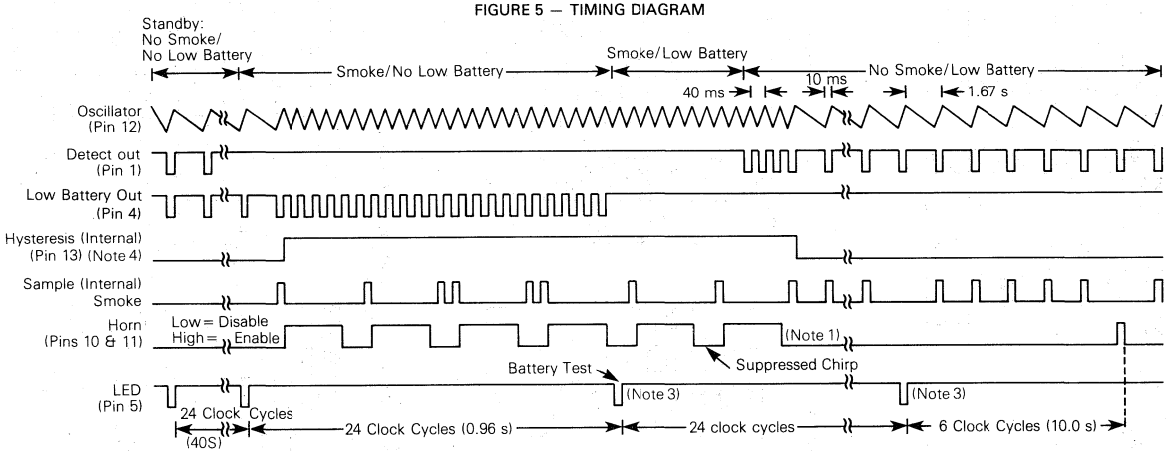
FIGURE 5 — TIMING DIAGRAM



NOTES: 1. Horn modulation is self-completing. When going from smoke to no smoke, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no smoke, 40 ms for smoke).
3. Low battery comparator information is latched only during LED pulse.
4. ~ 100 mV p-p swing.

MOTOROLA

MC14468

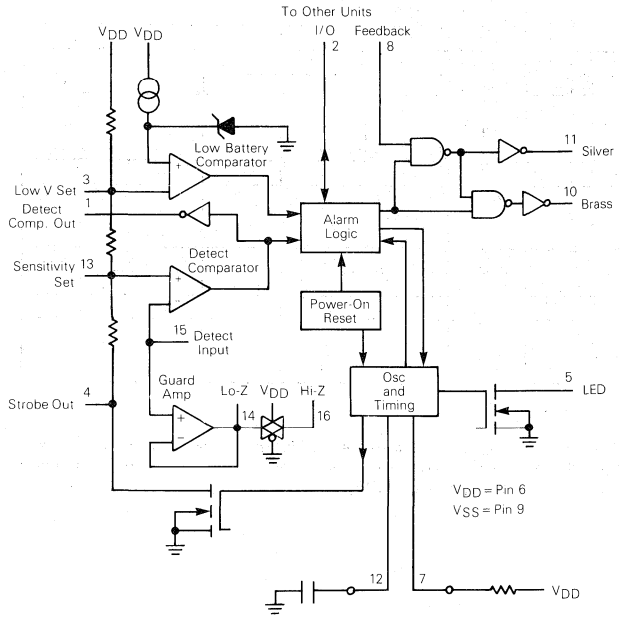
Advance Information

LOW-COST SMOKE DETECTOR WITH INTERCONNECT

The MC14468, when used with an ionization chamber and a small number of external components, will detect smoke. When smoke is sensed, an alarm is sounded via an external piezoelectric transducer and internal drivers. This circuit is designed to comply with the UL217 specification.

- Ionization Type with On-Chip FET Input Comparator
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Input-Protection Diodes on the Detect Input
- Low-Battery Trip Point, Internally Set, Can Be Altered Via External Resistor
- Detect Threshold, Internally Set, Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Output for Detect
- Internal Reverse Battery Protection
- Strobe Output for External Trim Resistors
- I/O Pin Allows Up to 40 Units to be Connected for Common Signaling
- Power-On Reset Prevents False Alarms on Battery Change

BLOCK DIAGRAM



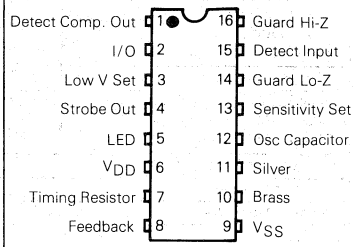
CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

LOW-COST SMOKE DETECTOR WITH INTERCONNECT

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs Except Pin 8	V_{in}	−0.25 to V_{DD} +0.25	V
DC Current Drain per Input Pin, Except Pin 15 = 1 mA	I	10	mA
DC Current Drain per Output Pin	I	30	mA
Operating Temperature Range	T_A	−10 to +60	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Reverse Battery Time	t_{RB}	5.0	s

*Maximum Ratings are those values beyond which damage to the device may occur.

RECOMMENDED DC OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	9.0	V
Timing Capacitor	–	0.1	μF
Timing Resistor	–	8.2	MΩ
Battery Load (Resistor or LED)	–	10	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic		Symbol	V_{DD} V_{dc}	Min	Typ	Max	Unit
Operating Voltage		V_{DD}	–	6.0	–	12	V
Output Voltage		V_{OH}					V
Piezoelectric Horn Drivers (I_{OH} = −16 mA)			7.2	6.3	–	–	
Comparators (I_{OH} = −30 μA)			9.0	8.5	8.8		
Piezoelectric Horn Drivers (I_{OL} = +16 mA)		V_{OL}	7.2	–	–	0.9	V
Comparators (I_{OL} = +30 μA)			9.0	–	0.1	0.5	
Output Voltage – LED Driver, I_{OL} = 10 mA		V_{OL}	7.2	–	–	3.0	V
Output Impedance, Active Guard	Pin 14	Lo-Z	9.0	–	10	–	kΩ
	Pin 16	Hi-Z	9.0	–	500	–	
Operating Current (R_{bias} = 8.2 MΩ)		I_{DD}	9.0	–	5.0	9.0	μA
			12.0	–	–	12.0	
Input Current – Detect (40% R.H.)		I_{in}	9.0	–	–	±1.0	pA
Input Current, Pin 8		I_{in}	9.0	–	–	±0.1	μA
Input Current @ 50°C, Pin 15		I_{in}	–	–	–	±6.0	pA
Internal Set Voltage							
Low Battery		V_{low}	9.0	7.2	–	7.8	V
Sensitivity		V_{set}	–	47	50	53	%V_{DD}
Hysteresis		V_{hys}	9.0	75	100	150	mV
Offset Voltage (measured at V_{in} = V_{DD}/2)		V_{OS}					mV
Active Guard			9.0	–	–	±100	
Detect Comparator			9.0	–	–	±50	
Input Voltage Range, Pin 8		V_{in}	–	−10	–	V_{DD} + 10	V
Input Capacitance		C_{in}	–	–	5.0	–	pF
Common Mode Voltage Range, Pin 15		V_{cm}	–	0.6	–	V_{DD} − 2	V
I/O Current, Pin 2							μA
Input, V_{OL} = V_{DD} − 2		I_{OL}	–	25	–	100	
Output, V_{OH} = V_{DD} − 2		I_{OH}	–	−4.0	–	−16	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

TIMING PARAMETERS ($C = 0.1\ \mu F$, $R_{Bias} = 8.2\ M\Omega$, $V_{DD} = 9.0$ V, $T_A = 25°C$, See Figure 5)

Characteristics		Symbol	Min	Typ	Max	Units
Oscillator Period	No Smoke	t_{Cl}	1.34	1.67	2.0	s
	Smoke		32	40	48	ms
Oscillator Rise Time		t_r	8	10	12	ms
Horn Output	On Time	PW_{on}	120	160	208	ms
(During Smoke)	Off Time	PW_{off}	60	80	104	ms
LED Output	Between Pulses	t_{LED}	32	40	48	s
	On Time	PW_{on}	8	10	12	ms
Horn Output	On Time	t_{on}	8	10	12	ms
(During Low Battery)	Between Pulses	t_{off}	32	40	48	s

FIGURE 1 — TYPICAL LED OUTPUT I-V CHARACTERISTIC

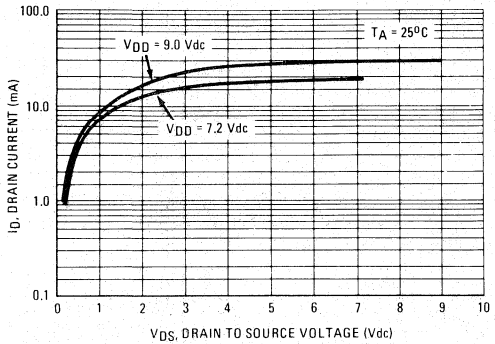


FIGURE 2 — TYPICAL COMPARATOR OUTPUT I-V CHARACTERISTIC

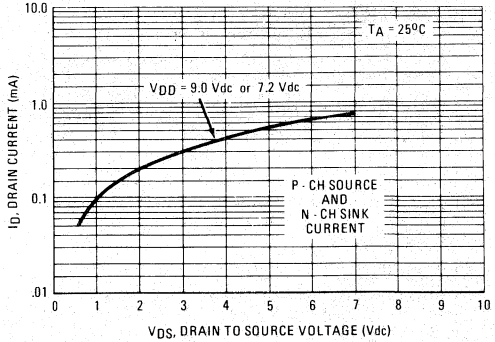
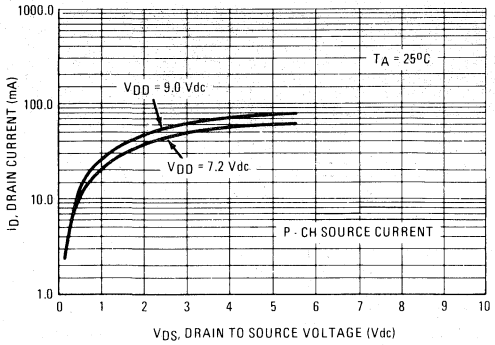
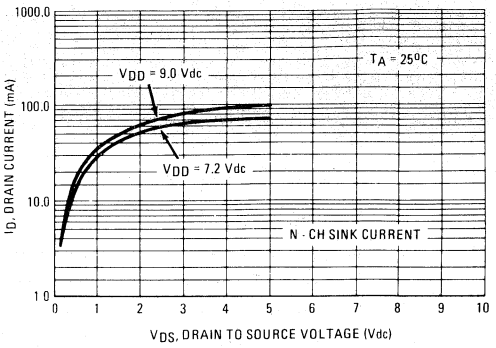


FIGURE 3 — TYPICAL P HORN DRIVER OUTPUT I-V CHARACTERISTIC





8

DEVICE OPERATION

TIMING

The internal oscillator of the MC14468 operates with a period of 1.67 seconds during no-smoke conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for smoke, except during LED pulse, Low Battery Alarm Chirp, or Horn Modulation (in smoke). Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage. Since very small currents are used in the oscillator, the oscillator capacitor should be of a low leakage type.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 160 ms on, 80 ms off. During the off time, smoke is again checked and will inhibit further horn output if no smoke is sensed. During local smoke conditions the low battery alarm is inhibited, but the LED pulses at a 1.0 Hz rate. In remote smoke, the LED is inhibited as well.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins will be within 100 mV of the input signal. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. Pin 15 (the Detect input) has internal diode protection against static damage.

INTERCONNECT

The I/O (Pin 2), in combination with V_{SS}, is used to interconnect up to 40 remote units for common signaling. A Local Smoke condition activates a current limited output driver, thereby signaling Remote Smoke to interconnected units. A small current sink improves noise immunity during non-smoke conditions. Remote units at lower voltages do not draw excessive current from a sending unit at a higher voltage. The I/O is disabled for three oscillator cycles after power up, to eliminate false alarming of remote units when the battery is changed.

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider connected between V_{DD} and V_{SS}. These voltages can be altered by external resistors connected from pins 3 or 13 to either V_{DD} or V_{SS}. There will be a slight interaction here due to the common voltage divider network.

TEST MODE

Since the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level could be difficult and/or time-consuming. By forcing Pin 12 to V_{SS}, the power strobing is bypassed and the output, Pin 1, constantly shows smoke/no smoke. Pin 1 = V_{DD} for smoke. In this mode and during the 10 ms power strobe, chip current rises to approximately 50 μA.

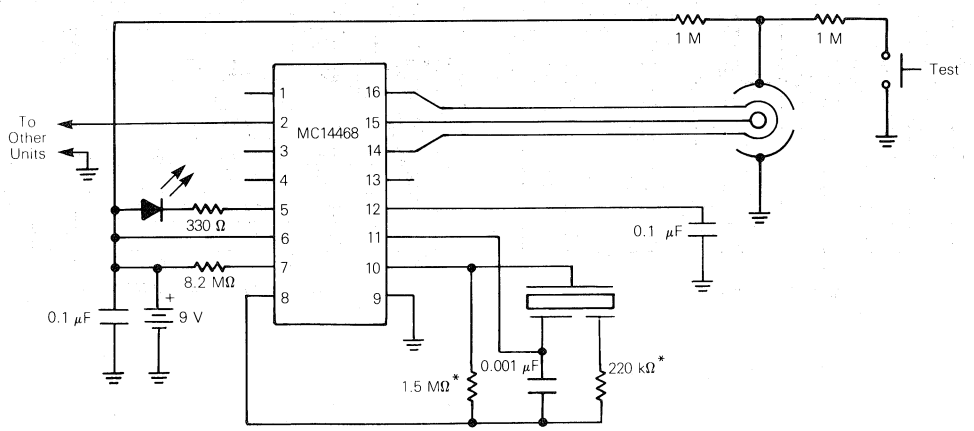
LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

HYSTERESIS

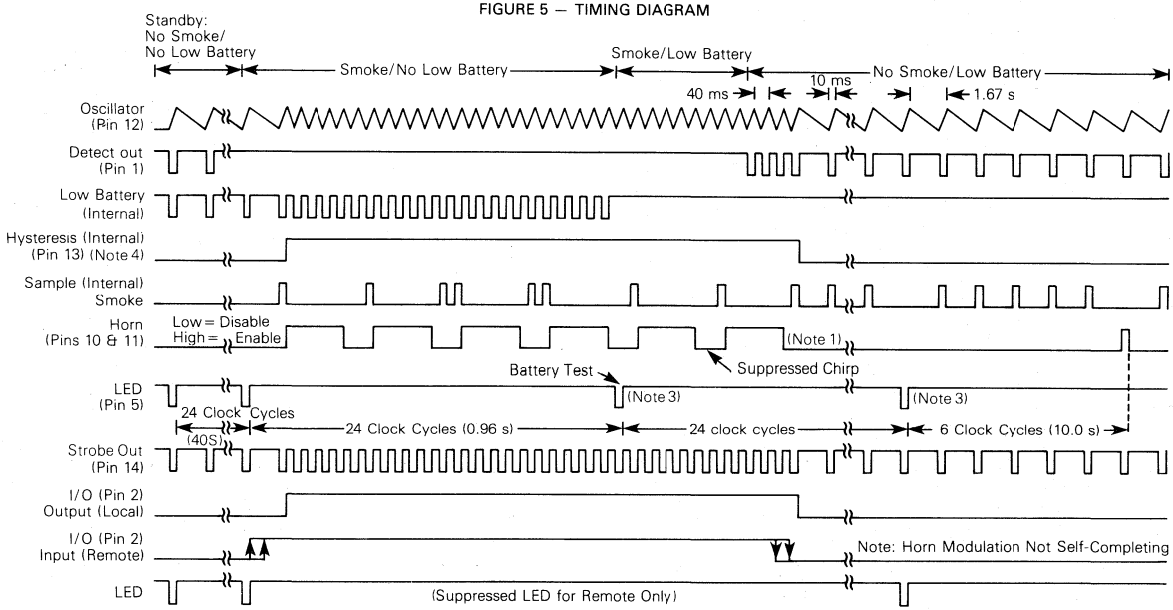
When smoke is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and reduces false triggering.

FIGURE 4 — TYPICAL APPLICATION AS IONIZATION SMOKE DETECTOR



*NOTE: Component values may change depending on type of piezoelectric horn used.

FIGURE 5 — TIMING DIAGRAM



NOTES: 1. Horn modulation is self-completing. When going from smoke to no smoke, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no smoke, 40 ms for smoke).
3. Low battery comparator information is latched only during LED pulse.
4. ~ 100 mV p-p swing.

Miscellaneous Functions

9

Device Number	Function
MC14460	Automotive Speed Control Processor
MC14490	Hex Contact Bounce Eliminator
MC14500B	Industrial Control Unit

MOTOROLA

MC14460

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

AUTOMOTIVE SPEED CONTROL PROCESSOR

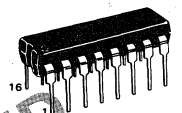
AUTOMOTIVE SPEED CONTROL PROCESSOR

The MC14460 device is designed to measure vehicle speed and provide pulse-width modulated outputs to trim a throttle positioning servo to maintain an internally stored reference speed.

The stored reference speed can be altered by the DECEL and ACCEL driver commands. The DECEL command trims down the speed, while ACCEL trims up the speed.

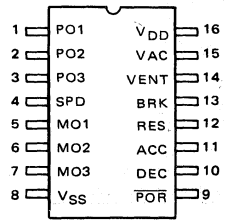
A BRAKE input is provided to turn off the outputs with a RESUME driver command to return the vehicle to the last stored speed.

- On-Chip Master Oscillator for System Time Reference
- Separate On-Chip Pulse Oscillator for Output Pulse Width Adjustment (Analogous to System Gain)
- Diode Protection on All Inputs
- Internal Redundant Brake and Minimum Speed Checks
- Acceleration Rates Controlled During ACCEL and RESUME Modes of Operation
- Low Frequency Speed Sensors Used
- No Throttle Position Feedback Required
- Power-On Reset
- Buffered Outputs Compatible with Discrete Transistor Driver Interface
- Low Power Dissipation

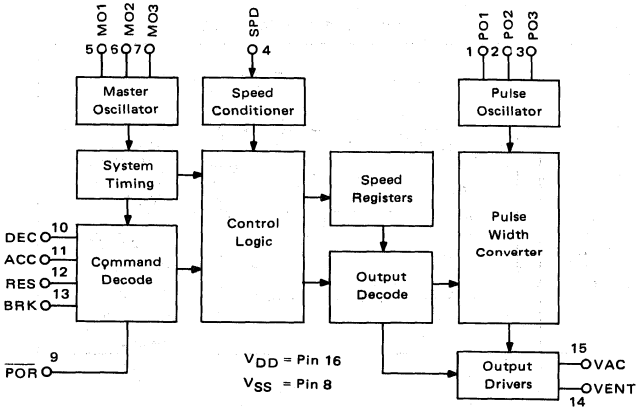


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

9

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Input Current, per Pin	I_{in}	±10	mAdc
Operating Temperature Range —	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Supply Voltage Pin 16	V_{DD}	—	4.0	5.0	6.0	Vdc
Output Voltage Pins 1, 2, 5, 6, 14, 15	V_{OL}	5.0	—	—	0.5	Vdc
	V_{OH}	5.0	4.5	—	—	Vdc
Input Voltage Pins 3, 7, 9, 10, 11, 12, 13	V_{IL}	—	—	—	0.3 V_{DD}	Vdc
	V_{IH}	—	0.7 V_{DD}	—	—	Vdc
Pin 4	V_{IL}	—	$\frac{V_{DD}}{2}$ -1.5	—	—	Vdc
	V_{IH}	—	—	—	$\frac{V_{DD}}{2}$ +1.5	Vdc
Input Hysteresis Pin 4 ($V_{IH} - V_{IL}$)	HYS	—	0.4	—	—	Vdc
Output Drive Current Pins 1, 2, 5, 6 V_{OH} = 4.6 Vdc	I_{OH}	5.0	-0.29	—	—	mAdc
V_{OL} = 0.4 Vdc	I_{OL}	5.0	+0.36	—	—	mAdc
Pins 14, 15 V_{OH} = 2.5 Vdc	I_{OH}	5.0	-2.0	—	—	mAdc
Input Current Pins 3, 4, 7, 10, 11, 12, 13 V_{IL} = 0.0 Vdc	I_{IL}	6.0	—	—	-1.0	μAdc
V_{OH} = 6.0 Vdc	I_{IH}	6.0	—	—	+1.0	μAdc
Pin 9 V_{IL} = 0.0 Vdc	I_{IL}	6.0	15	—	200	μAdc
V_{IH} = 6.0 Vdc	I_{IH}	6.0	—	—	+1.0	μAdc
Supply Current Pin 16 (Both Oscillators Active, VAC and VENT Outputs High)	I_{DD}	6.0	—	1.0	10	mAdc

FIGURE 1 — SYSTEM TIMING

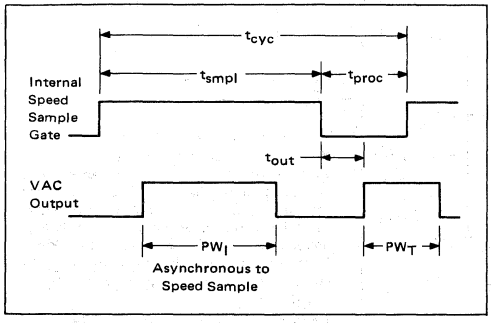
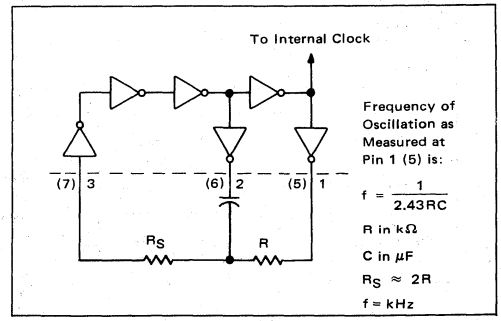


****FIGURE 2 — OSCILLATORS**



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SWITCHING CHARACTERISTICS (T_A = 25°C, V_{DD} = 4–6 Vdc)

Characteristics	Symbol	Min	Typ	Max	Unit
ACCEL Input Hold Time	t_{ACC}	$16/f_M$	9.52*	–	ms
DECEL Input Hold Time	t_{DEC}	$16/f_M$	9.52*	–	ms
RESUME Input Hold Time	t_{RES}	1	–	–	μs
BRAKE Input Hold Time	t_{BRK}	1	–	–	μs
Master Oscillator Frequency**					
T_A = -40°C to +85°C, R_S = 100 kΩ					
R = 43 kΩ, C = 5600 pF	f_M	1596	1680	1764	Hz
Useful Range		1344	1680	2016	Hz
Pulse Oscillator Frequency**					
T_A = -40°C to +85°C, R_S = 100 kΩ					
R = 43 kΩ, C = 5600 pF	f_P	1596	1680	1764	Hz
Useful Range		400	1600	3200	Hz
Speed Input Frequency	f_S	–	–	300	Hz
Speed Sample Time ($1008/f_M$)	t_{smpl}	–	600*	–	ms
Speed Processing Time ($16/f_M$)	t_{proc}	–	8.9*	–	ms
System Cycle Time ($1024/f_M$)	t_{cyc}	–	608.9*	–	ms
Output Delay Time ($9/f_M$)	t_{out}	–	5.4*	–	ms
Output Pulse Width					
Initializations (≈1/fp)	PW_I	280*	–	760*	ms
Trim Outputs (≈1/fp)	PW_T	10*	–	80*	ms

*f_M = 1680 Hz, f_P = 1600 Hz, f_S = 2.222 Hz/MPH

SYSTEM PERFORMANCE (T_A = 25°C, V_{DD} = 5 Vdc, f_M = 1680 Hz, f_S = 2.222 Hz/MPH)

Characteristic	Symbol	Typical	Unit
Speed Resolution ($f_M/2016\ f_S$)	S_{RES}	0.375	MPH
Minimum Operating Speed ($f_M/31.5\ f_S$)	S_{min}	24	MPH
Maximum Stored Speed ($f_M/8.4\ f_S$)	S_{max}	90	MPH
Controlled Acceleration Rate (ACCEL or RESUME Modes) $(f_M)^2/f_S\ (6.881)\ (10^5)$	A	1.85	MPH/s
Redundant Brake Speed Drop Below Stored Reference Speed $(-f_M/63\ f_S)$	S_{RB}	-12	MPH
Speed Deviation			
Assumes Suitable Mechanical Hookup and Pulse Oscillator Frequency Adjusted to Suit Throttle Servo Requirements			
Level Road (no wind, ±1% grades)	ΔS_N	±2	MPH
Transient Road Conditions (±10 MPH winds, ±7% grades)	ΔS_T	±3	MPH
Stored Speed Accuracy			
Steady-State (Acceleration = 0)	RS_{SS}	0.375	MPH
Transient (Acceleration = ±A MPH/s)	RS_T	0.6 A	MPH

TRUTH TABLE

OUTPUT		
VAC	VENT	SERVO DRIVE
0	0	Decrease Speed
0	1	Hold Speed
1	0	Invalid Output
1	1	Increase Speed

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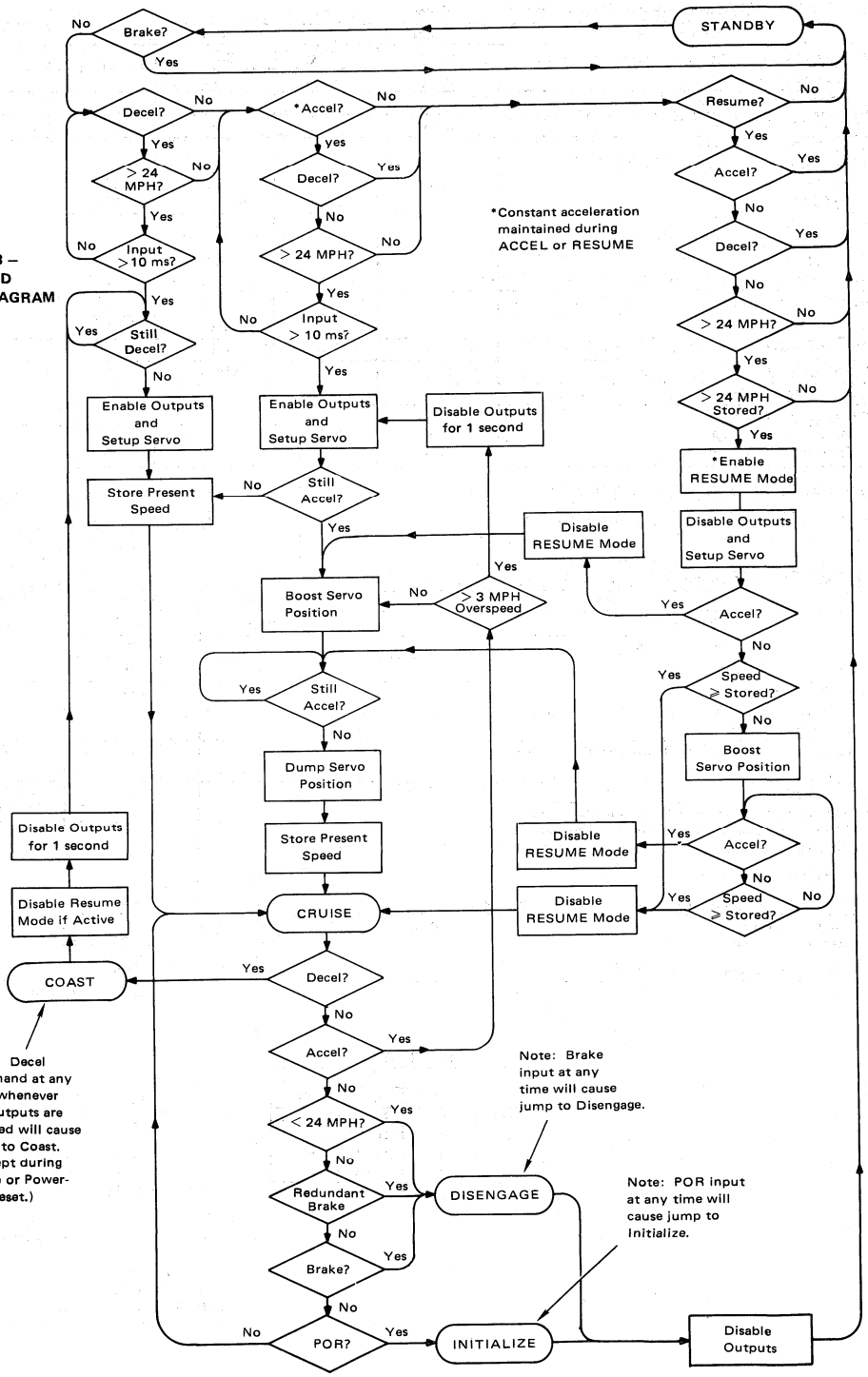


FIGURE 3 – COMMAND FLOW DIAGRAM

9

DEVICE OPERATION

PULSE OSCILLATOR (PO1, PO2, PO3; Pins 1, 2, 3)

These pins are the output pins of the output Pulse Oscillator, which is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the relative pulse width of the VAC and VENT outputs.

SPEED (SPD, Pin 4)

This is the Speed input to be controlled or stored. This input is level sensitive with hysteresis to allow use of slowly changing waveforms. Input frequency should never exceed 1/3 the Master Oscillator frequency (f_M).

MASTER OSCILLATOR (MO1, MO2, MO3; Pins 5, 6, 7)

The Master Oscillator is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the master system timing.

POWER-ON RESET (POR, Pin 9)

This pin is the Power-On Reset input. As long as this input is LOW, the internal system is cleared and the VAC and VENT outputs are disabled. An internal pullup device will source 15–200 μAdc of current from this pin to allow capacitor charging for automatic power-on reset.

DECEL (DEC, Pin 10)

This is the DECEL command input. When held HIGH both VAC and VENT outputs will be LOW. When the DECEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

ACCEL (ACC, Pin 11)

This is the ACCEL command input. When held HIGH the VAC and VENT outputs will be modulated to maintain a fixed rate of acceleration. When the ACCEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

continued

THROTTLE SERVO

A. Two Coil Vacuum Powered

Truth Table:

VAC Coil	VENT Coil	Throttle Action
Off	Off	Release
Off	On	Hold
On	Off	Weak Pull
On	On	Pull

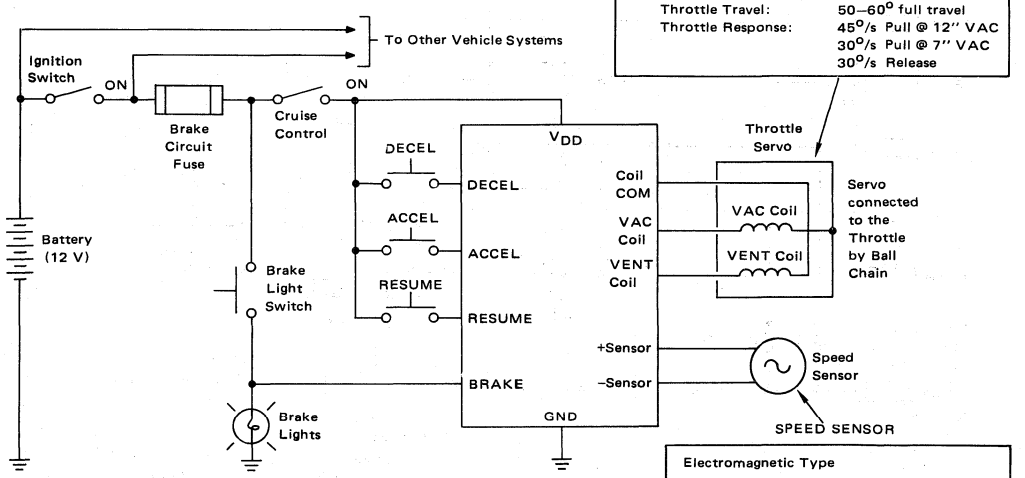
B. Coil Type

Coil Impedance: 80–90 Ω
Coil Inductance: 125–150 mH

C. Servo Response

Minimum Pulse Width: 5 ms
Throttle Travel: 50–60° full travel
Throttle Response: 45°/s Pull @ 12" VAC
30°/s Pull @ 7" VAC
30°/s Release

FIGURE 4 – TYPICAL AUTOMOTIVE CRUISE CONTROL APPLICATION



Electromagnetic Type

Poles:	8/revolution
Output Freq:	2.222 Hz/MPH (8000 pulses/mile)
Output Voltage:	> 3.0 Vp-p @ 24 MPH
Maximum Freq:	360 Hz (162 MPH)
DC Resistance:	< 40 Ω

9

DEVICE OPERATION continued

RESUME (RES, Pin 12)

This is the RESUME command input. When taken HIGH the system will lock into a mode where the VAC and VENT outputs are modulated to maintain a fixed rate acceleration. This acceleration ends when the SPD input sample matches the stored reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

BRAKE (BRK, Pin 13)

This is the BRAKE command input. When this input is taken HIGH the system is disabled (both VAC and VENT outputs LOW) until a DECEL, ACCEL, or RESUME command is received. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

VENT (Pin 14)

This is the VENT output. See Truth Table for operation.

VAC (Pin 15)

This is the VAC output. See Truth Table for operation.

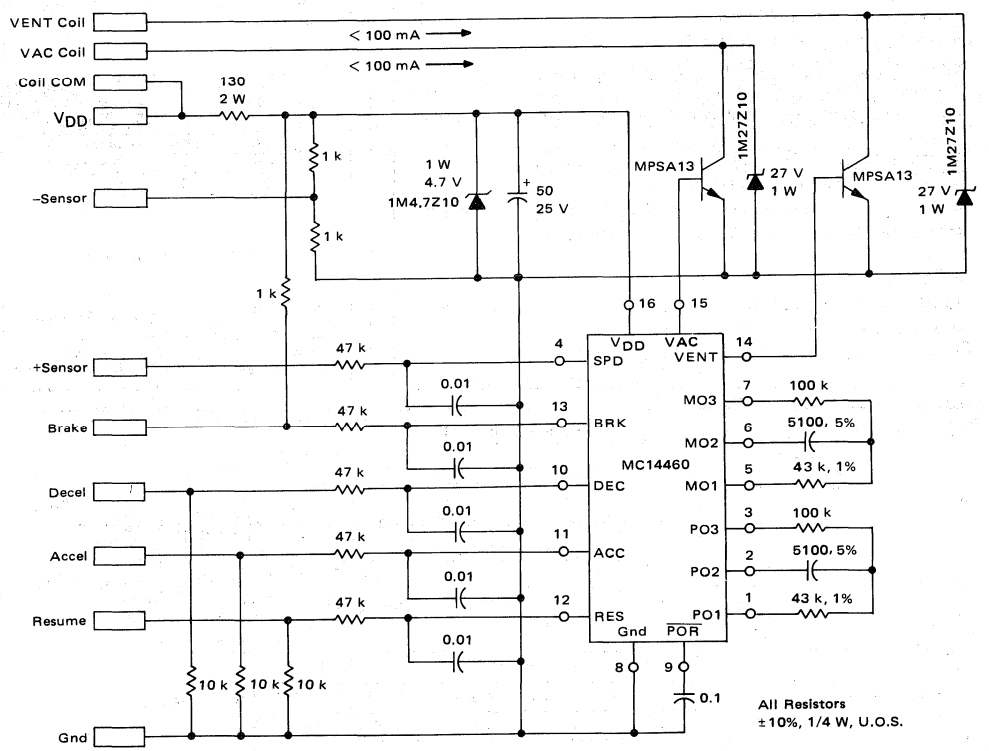
GROUND (V_{SS}, Pin 8)

Pin 8 is the ground connection for the package.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

Pin 16 is the power supply connection for the package.

FIGURE 5 – PC BOARD MODULE FOR CRUISE CONTROL



Environment

Ambient Temperature (T_A)	$-40^{\circ}C$ to $85^{\circ}C$
V_{CC} Operating Range	11–15 Vdc
V_{CC} Transients	9–16 Vdc
Load Dump	80 V Peak decaying to 12 V in < 200 ms
Inductive	±300 V Peak decaying in < 1 ms
Jump Start	+24 Vdc for 5 min.
Reverse Battery	−12 Vdc continuous

9

MOTOROLA

MC14490

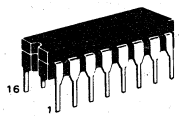
HEX CONTACT BOUNCE ELIMINATOR

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates

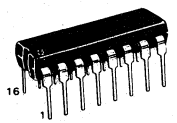
CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

HEX CONTACT BOUNCE ELIMINATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

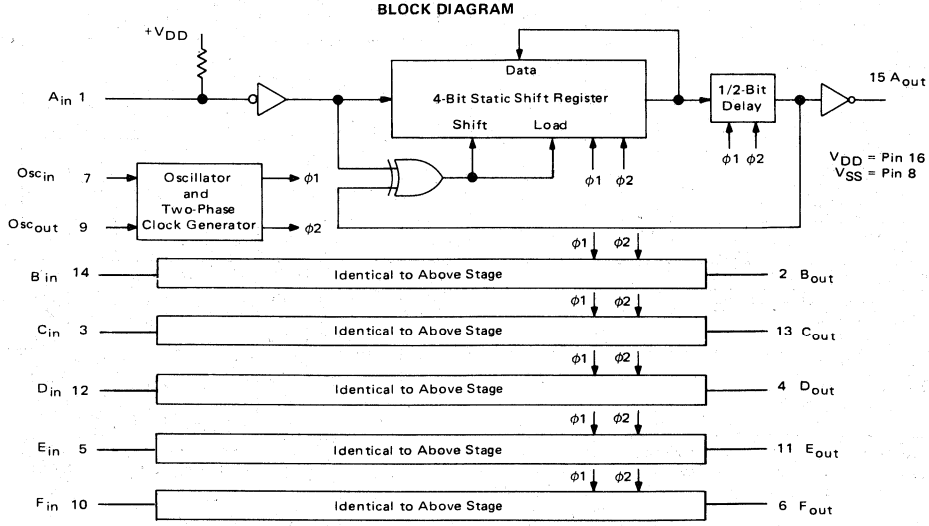
P SUFFIX
PLASTIC PACKAGE
CASE 648



ORDERING INFORMATION

MC14xxx	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package

BLOCK DIAGRAM



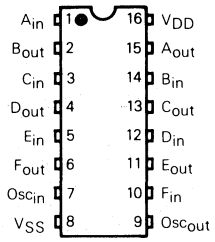
9

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage		V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs		V_{in}	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin		I_{in}	±10	mA
Operating Temperature Range	MC14490L MC14490P	T_A	−55 to +125 −50 to +85	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Power Dissipation, per Package†		P_D	500	mW

†Power Dissipation Temperature Derating
Plastic "P" Package – 12 mW/°C from 65 to 85°C
Ceramic "L" Package – 12 mW/°C from 100 to 125°C

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current	I_{OH}									mA
Source										
Oscillator Output										
(V_{OH} = 2.5 V)		5.0	−0.6	–	−0.5	−1.5	–	−0.4	–	
(V_{OH} = 4.6 V)		5.0	−0.12	–	−0.1	−0.3	–	−0.08	–	
(V_{OH} = 9.5 V)		10	−0.23	–	−0.20	−0.8	–	−0.16	–	
(V_{OH} = 13.5 V)		15	−1.4	–	−1.2	−3.0	–	−1.0	–	
Debounce Outputs										
(V_{OH} = 2.5 V)		5.0	−0.9	–	−0.75	−2.2	–	−0.6	–	
(V_{OH} = 4.6 V)		5.0	−0.19	–	−0.16	−0.46	–	−0.12	–	
(V_{OH} = 9.5 V)		10	−0.60	–	−0.50	−1.2	–	−0.4	–	
(V_{OH} = 13.5 V)		15	−1.8	–	−1.5	−4.5	–	−1.2	–	
Sink	I_{OL}									mA
Oscillator Output										
(V_{OL} = 0.4 V)		5.0	0.36	–	0.30	0.9	–	0.24	–	
(V_{OL} = 0.5 V)		10	0.9	–	0.75	2.3	–	0.6	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.5	10	–	2.8	–	
Debounce Outputs										
(V_{OL} = 0.4 V)		5.0	2.6	–	2.2	4.0	–	1.8	–	
(V_{OL} = 0.5 V)		10	4.0	–	3.3	9	–	2.7	–	
(V_{OL} = 1.5 V)		15	12	–	10	35	–	8.1	–	
Input Current	I_{IH}	15	–	2	–	0.2	2	–	11	μA
Debounce Inputs (V_{in} = V_{DD})										
Input Current Oscillator – Pin 7 (V_{in} = V_{SS} or V_{DD})	I_{in}	15	–	±620	–	±255	±400	–	±250	μA
Pullup Resistor Source Current	I_{IL}	5.0	210	375	140	190	255	70	130	μA
Debounce Inputs		10	415	740	280	380	500	145	265	
(V_{in} = V_{SS})		15	610	1100	415	570	750	215	400	
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{SS}	5.0	–	150	–	40	100	–	90	μA
(V_{in} = V_{SS} or V_{DD}, I_{out} = 0 μA)		10	–	280	–	90	225	–	180	
		15	–	840	–	225	650	–	550	

#Noise immunity specified for worst case combination.
Noise margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

*T_{low} = −55°C for L Device, −40° C for P Device.
T_{high} = +125°C for L Device, +85°C for P Device.

9

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time All Outputs	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time Oscillator Output	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Debounce Outputs	t_{THL}	5.0 10 15	– – –	60 30 20	120 60 40	
Propagation Delay Time Oscillator Input to Debounce Outputs	t_{PHL}	5.0 10 15	– – –	285 120 95	570 240 190	ns
	t_{PLH}	5.0 10 15	– – –	370 160 120	740 320 240	
Clock Frequency (50% Duty Cycle) (External Clock)	f_{cl}	5.0 10 15	– – –	2.8 6 9	1.4 3.0 4.5	MHz
Setup Time (See Figure 1)	t_{su}	5.0 10 15	100 80 60	50 40 30	– – –	ns
Maximum External Clock Input Rise and Fall Time Oscillator Input	t_r, t_f	5.0 10 15	No Limit			ns
Oscillator Frequency OSC_{out} $C_{ext} \geq 100$ pF*	f_{osc}, typ	5.0 10 15	$\frac{1.5}{C_{ext}\ (\text{in}\ \mu F)}$ $\frac{4.5}{C_{ext}\ (\text{in}\ \mu F)}$ $\frac{6.5}{C_{ext}\ (\text{in}\ \mu F)}$			Hz

***POWER-DOWN CONSIDERATIONS**

Large values of C_{ext} may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA; therefore the turn-off time of the power supply must not be faster than $t = (V_{DD} - V_{SS}) \cdot C_{ext}/(10\ mA)$. For example, if $V_{DD} - V_{SS} = 15$ V and $C_{ext} = 1\ \mu F$, the power supply must turn off no faster than $t = (15\ V) \cdot (1\ \mu F)/10\ mA = 1.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

FIGURE 1 — SWITCHING WAVEFORMS

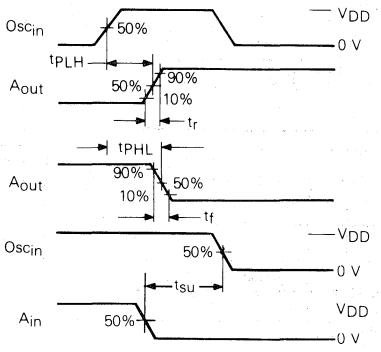
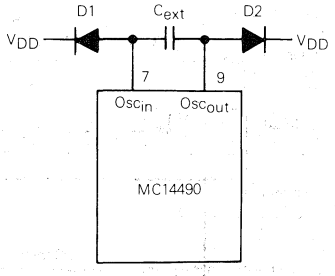


FIGURE 2 — DISCHARGE PROTECTION DURING POWER DOWN



9

THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4½-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open, (see Figure 4) the high level is inverted, and the shift register is loaded with a low on each negative edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the negative edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a 3½ to 4½ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+1 a low is loaded into the first bit. Just after N+1, when the input bounces low, all bits are set to a high. At N+2 nothing happens because the input and output are low and all bits of the shift register are high. At time N+3 and thereafter the input signal is a high, clean signal. At the positive edge of N+6 the output goes high as a result of four lows being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

FIGURE 3 — TIMING DIAGRAM

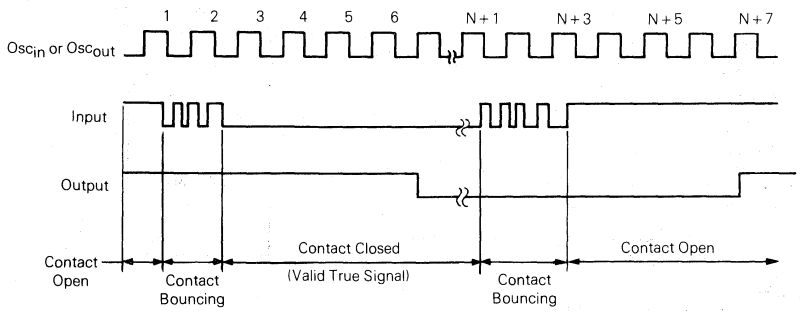
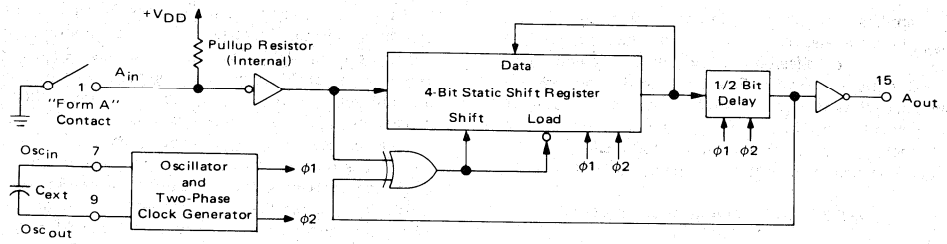


FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

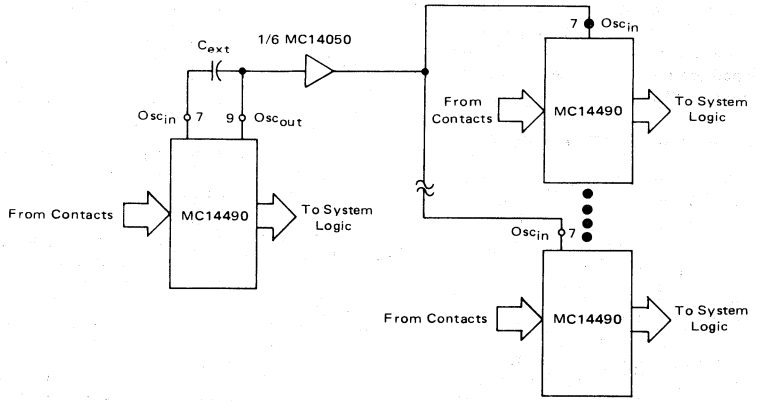
The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR
DEBOUNCE SYSTEM

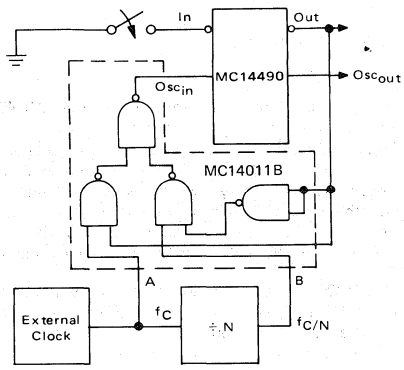


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

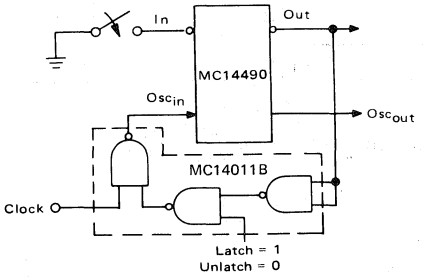
FIGURE 6 – FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 – LATCHED OUTPUT CIRCUIT



MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $\overline{A}B$ as shown in Figures 9 and 10. The signal $\overline{A}B$ is four clock periods in length. If the inverter is switched to the A output, the pulse $A\overline{B}$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 – MULTIPLE TIMING CIRCUIT CONNECTIONS

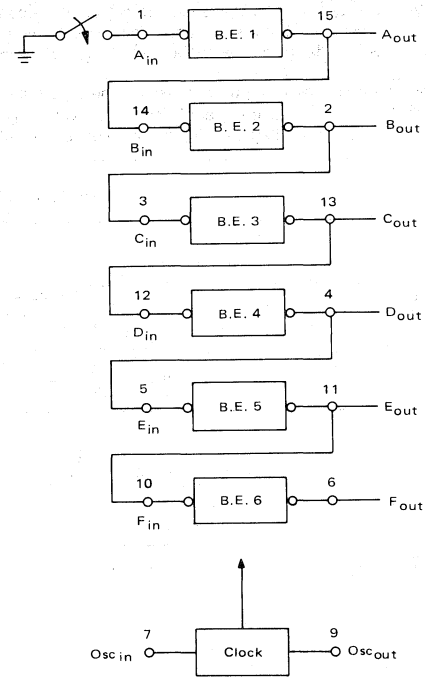


FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT

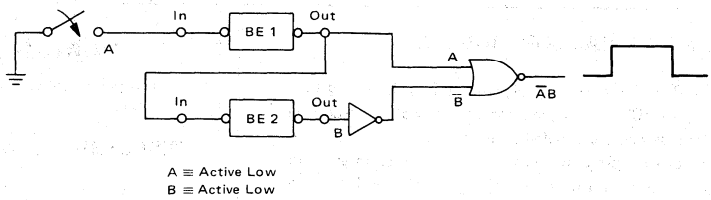
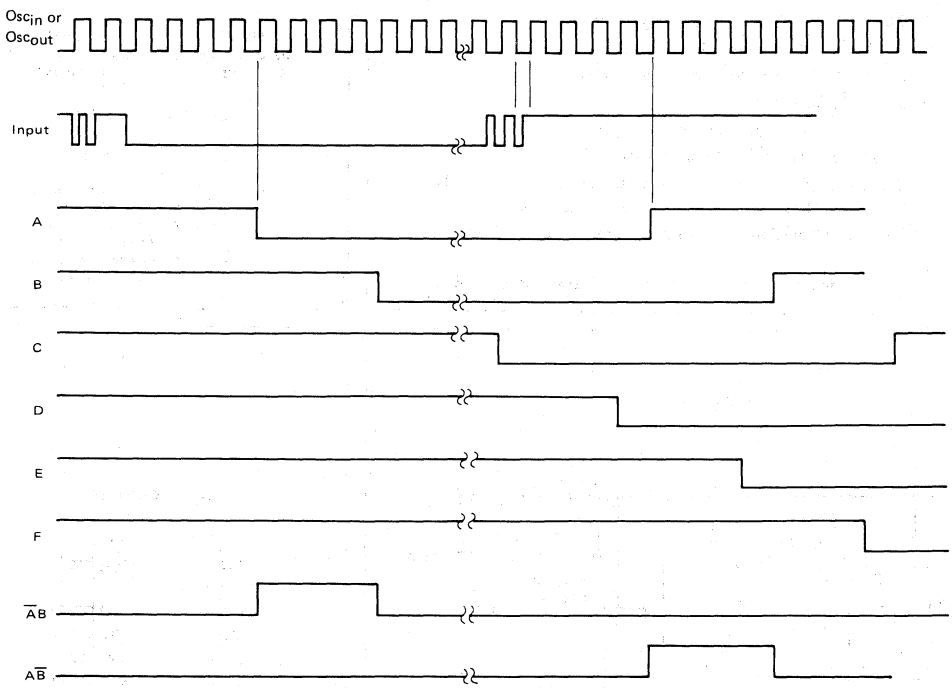


FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

9

MOTOROLA

MC14500B

INDUSTRIAL CONTROL UNIT

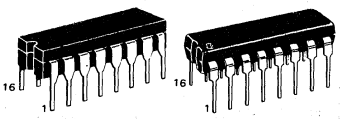
The MC14500B Industrial Control Unit (ICU) is a single-bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single-bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored-program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

- 16 Instructions
- DC to 1.0 MHz Operation at V_{DD} = 5 V
- On-Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 to 18 V Operation
- Noise Immunity Typically 45% of V_{DD}
- Low Quiescent Current Characteristic of CMOS Devices
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range
- Detailed Operation and Applications Given in Handbook HB-209
- Development System Described in Application Note AN-889

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL CONTROL UNIT



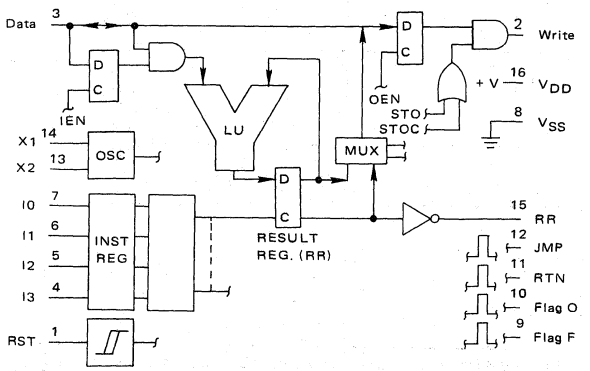
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

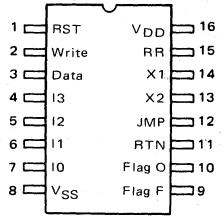
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



PIN ASSIGNMENT



9

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			V	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
$V_{in} = 0$ or V_{DD}	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage	"0" Level	V_{IL}									V
RST, D, X2											
(V_O = 4.5 or 0.5 V)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 V)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)			15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage #	"0" Level	V_{IL}									V
I0, I1, I2, I3											
(V_O = 4.5 or 0.5 V)			5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 V)			10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 V)			15	–	2.4	–	3.4	2.4	–	2.4	
	"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 V)			5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 V)			10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 V)			15	10	–	10	4.3	–	10	–	
Output Drive Current	Source	I_{OH}									mA
Data, Write (AL/CL/CP Device)											
(V_{OH} = 4.6 V)			5.0	−1.2	–	−1.0	-2.0	–	−0.7	–	
(V_{OH} = 9.5 V)			10	−3.6	–	−3.0	-6.0	–	−2.1	–	
(V_{OH} = 13.5 V)			15	−7.2	–	−6.0	-12	–	−4.2	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	1.9	–	1.6	3.2	–	1.1	–	
(V_{OL} = 0.5 V)			10	3.6	–	3.0	6.0	–	2.1	–	
(V_{OL} = 1.5 V)			15	7.2	–	6.0	12	–	4.2	–	
Output Drive Current	Source	I_{OH}									mA
Other Outputs (AL Device)											
(V_{OH} = 2.5 V)			5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 V)			5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 V)			10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 V)			15	-4.2	–	-3.4	8.8	–	-2.4	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 V)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current	Source	I_{OH}									mA
Other Outputs (CL/CP Device)											
(V_{OH} = 2.5 V)			5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 V)			5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 V)			10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 V)			15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	3.6	–	3.0	8.8	–	2.4	–	

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ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	V_{DD} V	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current, RST (AL/CL/CP Device)	I_{in}	15	25	—	—	150	—	—	250	μA
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance (Data)	C_{in}	—	—	—	—	15	—	—	—	pF
Input Capacitance (All Other Inputs)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package) I_{out} = 0 μA, V_{in}=0 or V_{DD}	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Quiescent Current (CL/CP Device) (Per Package) I_{out} = 0 μA, V_{in}=0 or V_{DD}	I_{DD}	5.0 10 15	— — —	20 40 80	— — —	0.005 0.010 0.015	20 40 80	— — —	150 300 600	μA
**Total Supply Current at an External Load Capacitance (C_L) on All Outputs	I_T	—	I_T = (1.5 μA/kHz) f + I_{DD} I_T = (3.0 μA/kHz) f + I_{DD} I_T = (4.5 μA/kHz) f + I_{DD}							μA

* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
** The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (T_A = 25°C; t_r = t_f = 20 ns for X and I inputs; C_L = 50 pF for JMP, X1, RR, Flag O, Flag F; C_L = 130 pF + 1 TTL load for Data and Write.)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ	All Types Max	Unit
Propagation Delay Time, X1 to RR	t_{PLH}, t_{PHL}	5.0	—	250	500	ns
		10	—	125	250	
		15	—	100	200	
X1 to Flag F, Flag O, RTN, JMP		5.0	—	200	400	
		10	—	100	200	
		15	—	85	170	
X1 to Write		5.0	—	225	450	
		10	—	125	250	
		15	—	100	200	
X1 to Data		5.0	—	250	500	
		10	—	120	240	
		15	—	100	200	
RST to RR		5.0	—	250	500	
		10	—	125	250	
		15	—	100	200	
RST to X1		5.0	—	450	Note 1	
		10	—	200		
		15	—	150		
RST to Flag F, Flag O, RTN, JMP		5.0	—	400	800	
		10	—	200	400	
		15	—	150	300	
RST to Write, Data		5.0	—	450	900	
		10	—	225	450	
		15	—	175	350	
Clock Pulse Width, X1	$t_{W(cl)}$	5.0	400	200	—	ns
		10	200	100	—	
		15	180	90	—	
Reset Pulse Width, RST	$t_{W(R)}$	5.0	500	250	—	ns
		10	250	125	—	
		15	200	100	—	
Setup Time — Instruction	$t_{su(I)}$	5.0	400	200	—	ns
		10	250	125	—	
		15	180	90	—	
Data	$t_{su(D)}$	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	
Hold Time — Instruction	$t_{h(I)}$	5.0	100	0	—	ns
		10	50	0	—	
		15	50	0	—	
Data	$t_{h(D)}$	5.0	200	100	—	ns
		10	100	50	—	
		15	100	50	—	

NOTE 1. Maximum Reset Delay may extend to one-half clock period.

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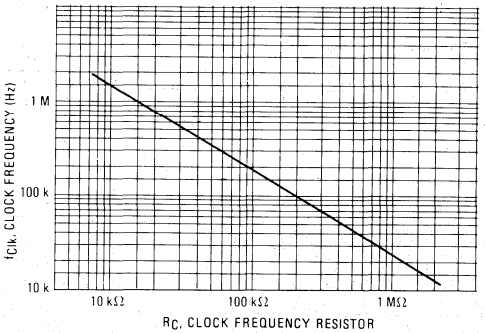
FIGURE 1 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

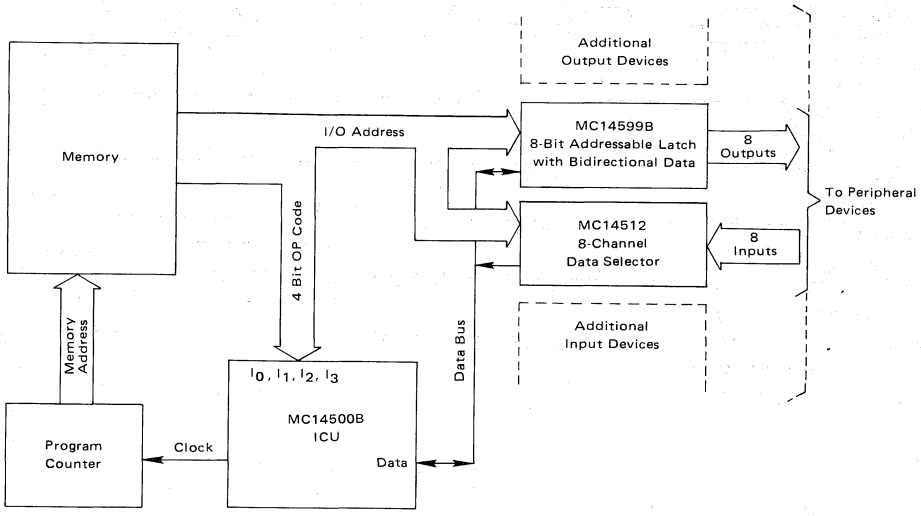


Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	I_3
5	Bit 2 Instruction Word	I_2
6	Bit 1 Instruction Word	I_1
7	LSB Instruction Word	I_0
8	Negative Supply (Ground)	V_{SS}
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

TABLE 1. MC14500B INSTRUCTION SET

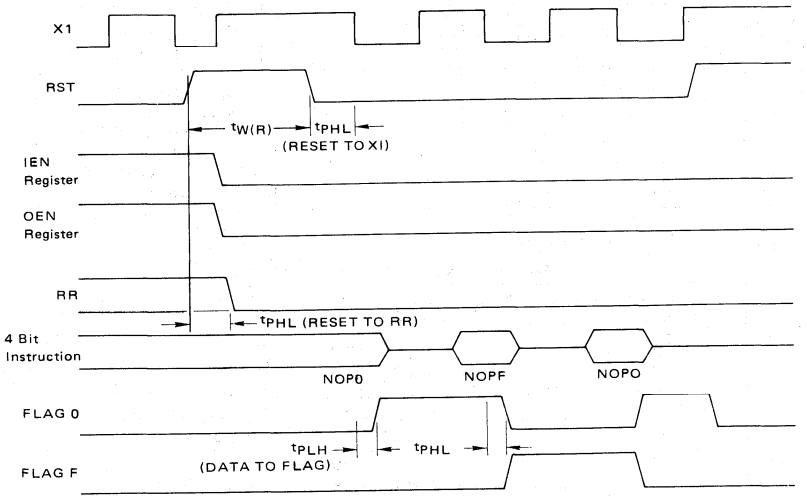
Instruction Code	Mnemonic	Action
0 0000	NOPO	No change in registers. RR → RR, Flag O → ⎍
1 0001	LD	Load result register. Data → RR
2 0010	LDC	Load complement. $\overline{Data}$ → RR
3 0011	AND	Logical AND. RR·Data → RR
4 0100	ANDC	Logical AND complement. RR·$\overline{Data}$ → RR
5 0101	OR	Logical OR. RR + Data → RR
6 0110	ORC	Logical OR complement. RR + $\overline{Data}$ → RR
7 0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8 1000	STO	Store. RR → Data Pin, Write → ⎍
9 1001	STOC	Store complement. $\overline{RR}$ → Data Pin, Write → ⎍
A 1010	IEN	Input enable. Data → IEN Register
B 1011	OEN	Output enable. Data → OEN Register
C 1100	JMP	Jump. JMP Flag → ⎍
D 1101	RTN	Return. RTN Flag → ⎍ and skip next instruction
E 1110	SKZ	Skip next instruction if RR = 0
F 1111	NOPF	No change in registers. RR → RR, Flag F → ⎍

FIGURE 2 – OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM

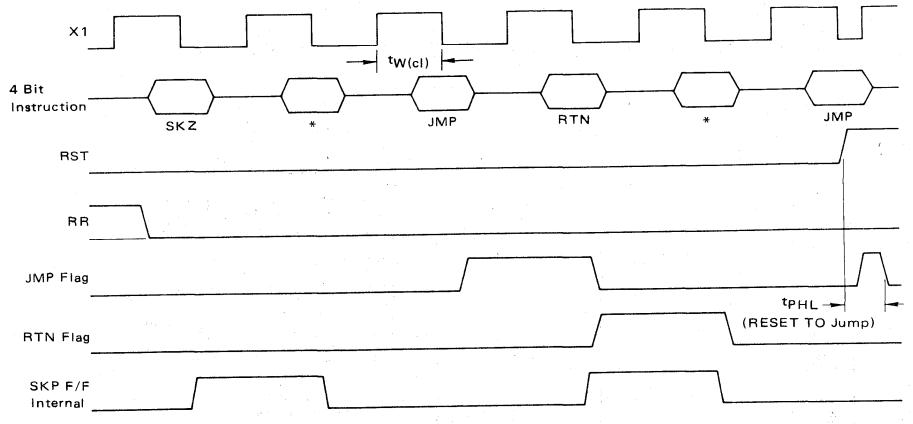


TIMING WAVEFORMS

Instructions NOPO, NOPF
RR, IEN, OEN remain unaffected



Instructions SKZ, JMP, RTN
RR, IEN, OEN remain unaffected



* Instructions Ignored.

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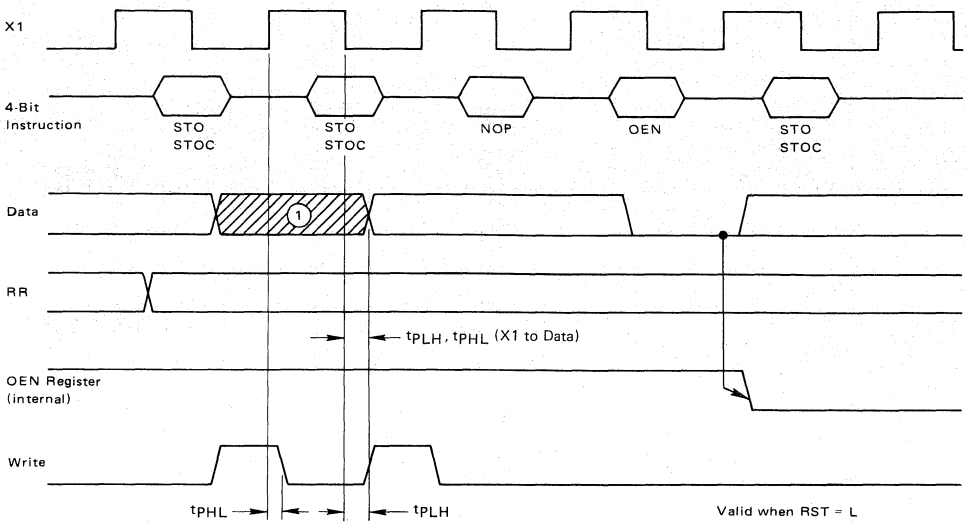
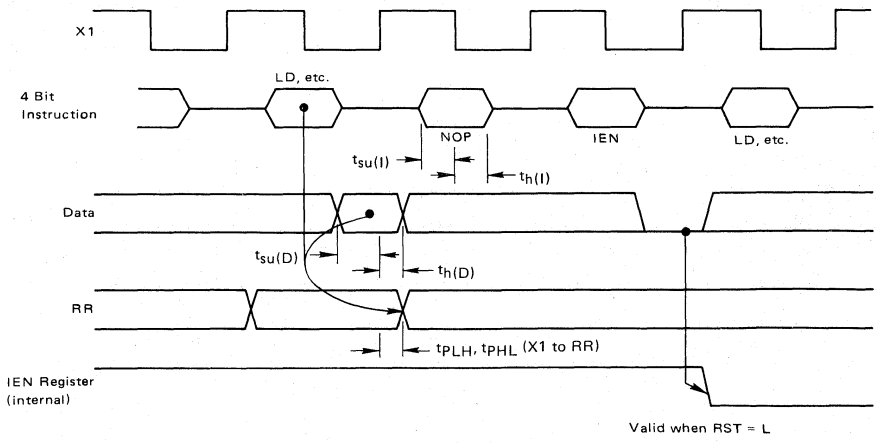
TIMING WAVEFORMS

Instructions STO, STOC, OEN



NOTE 1. Valid output data.

Instructions LD, LDC, AND, ANDC OR, ORC, XNOR, IEN



Reliability 10

MOTOROLA

Introduction

This chapter is intended to demonstrate the quality and reliability aspects of the semiconductor products supplied by Motorola.

Quality in Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is its philosophy to "design in" reliability. At all development points of any new design reliability orientated guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola Incoming Inspection Specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

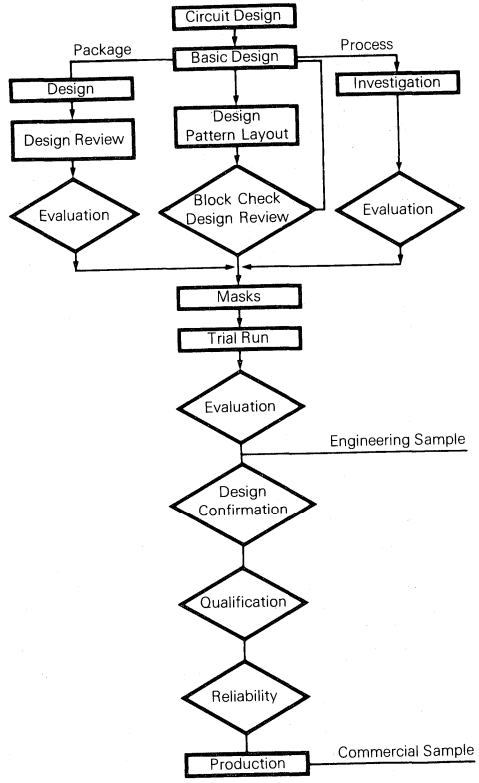
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



This basic design flow-chart omits some feedback loops for simplicity

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WAFER FABRICATION

All processing stages of Motorola products are subjected to demanding manufacturing and quality control standards. A philosophy of "Do it Right the First Time" is instrumental in assuring that Motorola has a reliability record second to none.

The Bipolar and MOS Wafer Fabrication flow charts are examples which highlight the various in process control points audited by both Manufacturing and Quality people. The majority of these inspections are control audit points with inspection gates at critical points of the process; this is in line with Motorola policy of all personnel being responsible for quality at each manufacturing stage.

Diffusion and ion implantation processing is subject to oxide thickness controls penetration evaluations. Controls are also performed on resistivity and defect density. Diffusion furnaces, metallization, and passivation equipment are subjected to daily qualification requirements by using C-V plotting techniques. C-V techniques are also used to ensure ongoing stability as they do provide a very sensitive measurement of ionic species concentration.

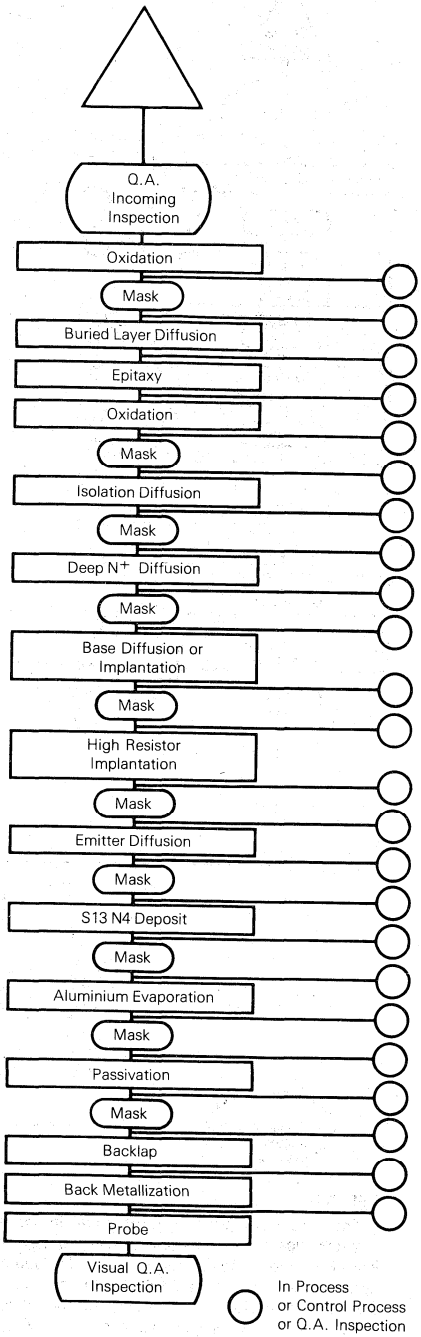
In addition many other specific controls are used as a means to ensure built-in reliability and provide statistical trend data, which include:

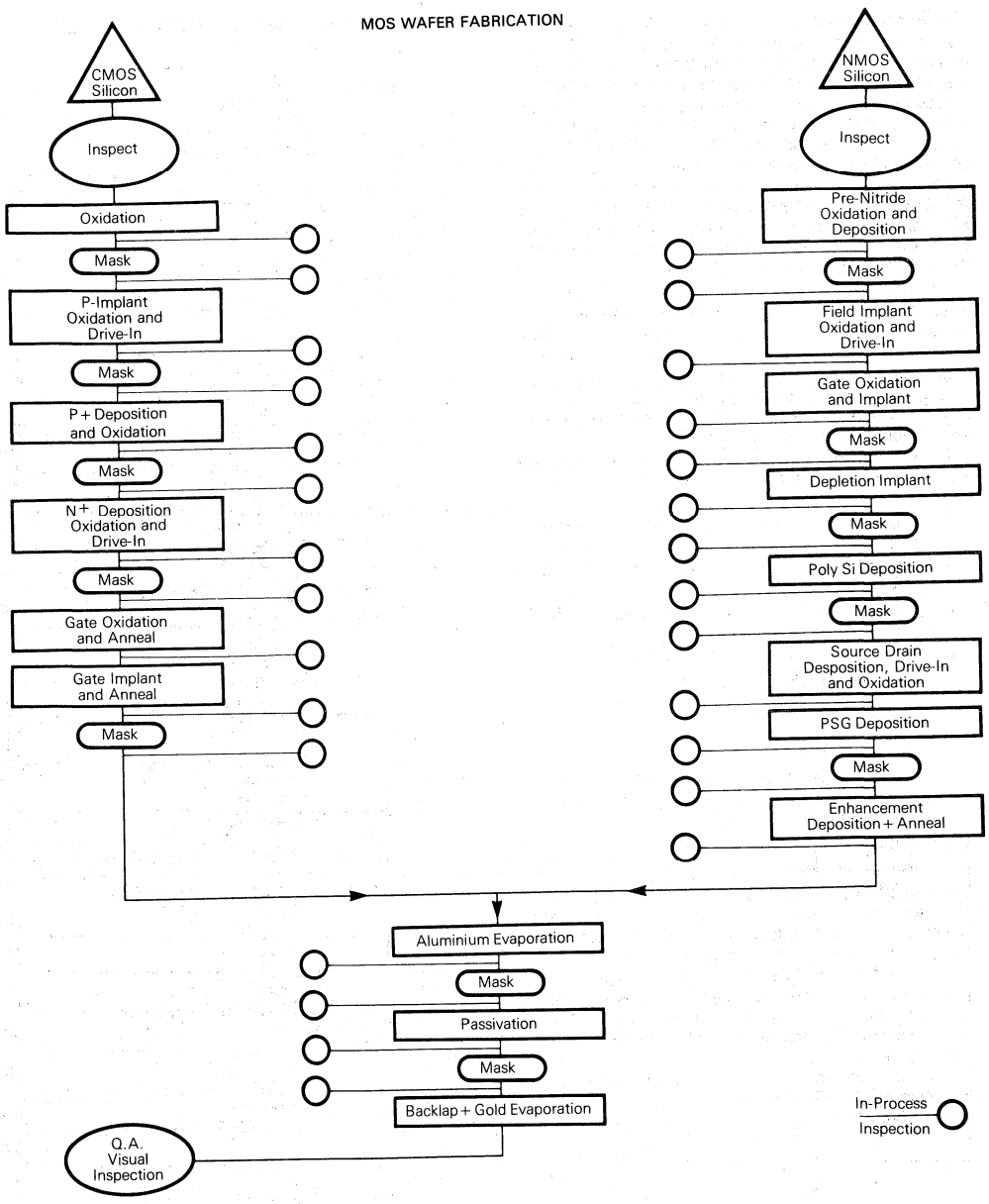
- Environmental monitoring for humidity, temperature and particles
- Deionized water resistivity, particles and bacteria checks in water
- Epitaxial material: resistivity — thickness — crystal defects
- Oxide: thickness — charges — pinhole density
- Metallization: thickness — adherence — metal composition — ohmic contacts
- Doping profiles
- Pre and post etch inspections
- In process SEM analysis for step coverage: metallization — grain size — phosphorous concentration
- Passivation integrity checks
- Calibration
- Final visual inspection gate.

After all processing stages are completed, every wafer lot is subject to a detailed electrical parameter check. Parameters such as threshold voltage, junction breakdown voltages, resistivity, field inversion voltages, etc., are measured and each batch is sentenced accordingly. The data generated at this point is treated statistically as a control on the distribution of each key electrical parameter thus allowing corrective action adjustments to be implemented in a timely manner.

Every wafer lot is submitted to an electrical probe test during which every individual die is tested to its electrical specification. Chips which fail are individually inked.

BIPOLAR WAFER FABRICATION





ASSEMBLY

The assembly operation is of equal importance to the wafer fabrication process as a manufacturing activity which will effect the reliability of the finished product. Motorola continuously makes major investments in specialized assembly areas located in Malaysia, the Philippines and Korea. These assembly plants employ the latest technologies available to ensure that all Motorola semiconductors are produced to the highest standards of Quality and Reliability. In addition, each wafer fabrication facility has in-house assembly capability which allows some production, specific engineering activity and qualification of piece-parts suppliers. The major production volumes of Motorola's Integrated Circuits are assembled offshore in the Far East.

identical Quality and Reliability philosophies are practiced in the assembly areas as within the wafer fabrication facilities. Quality Assurance Audits for immediate corrective actions are performed after major process steps as demonstrated in the flow-chart. In addition, screening options are available. The statistical data obtained from quality audits are reported to the appropriate business centers either daily, weekly or monthly for review.

Motorola is particularly aware of the major impact moisture can have on the reliability performance of either plastic or ceramic parts. With this in mind several major new innovations have been introduced to safeguard Motorola products and thus enhance their overall reliability performance, these include:

- Faraday shield vacuum packed wafer shipping system
- Temperature and humidity controlled wafer inventory stores
- Inert atmosphere for metal can packages encapsulation
- New design lead frames (plastic assembly)
- New molding compounds
- Low moisture content glass
- Moisture content audit procedures
- Super dry piece-part controls

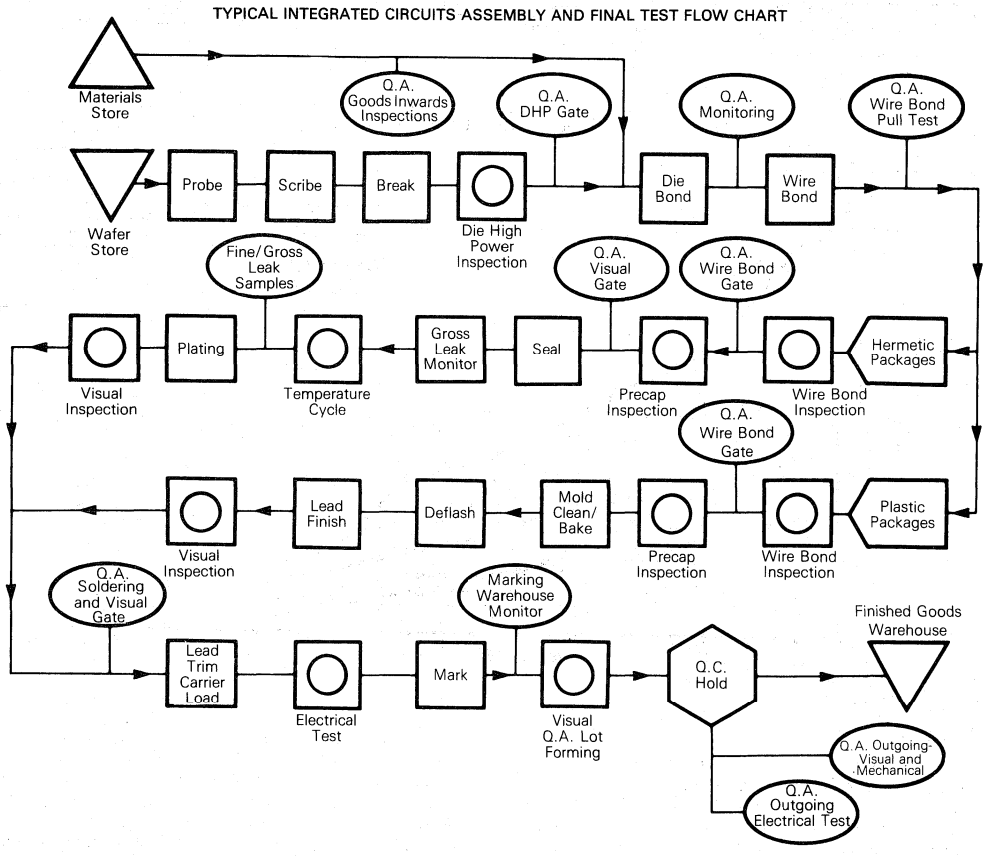
FINAL TESTING

Each of Motorola's facilties has a complete Final Test capability for all of the products fabricated and assembled. The majority of products, after assembly, are tested and Q.A. released at the facility responsible for that product. Some product is tested in the offshore assembly site; however, this is always returned to the facility for Q.A. release prior to final shipment to customer.

Final Test is a comprehensive series of dc, functional and speed orientated electrical tests as well as adapted forced tests. These tests are normally more stringent than data sheet requirements and are finally sampled by Outgoing Quality Assurance.

In practice, the test flow philosophies vary according to product. For instance, most of the Discrete devices are double tested as part of a zero defect quality improvement program. As well, many Integrated Circuits are tested at various temperatures. There are also many burn-in options available.

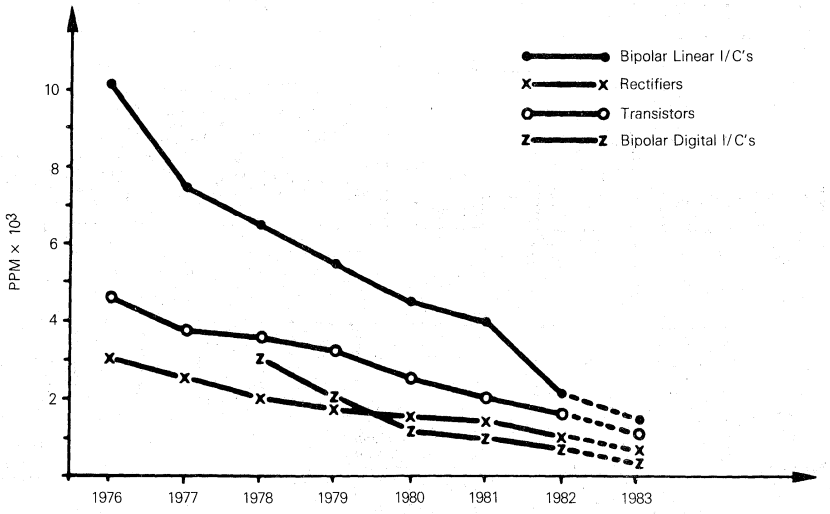
TYPICAL INTEGRATED CIRCUITS ASSEMBLY AND FINAL TEST FLOW CHART



OUTGOING QUALITY SAMPLING PLAN

		A.Q.L. 1979	1980	1981	1982	1983
Rectifiers	Electrical Inoperative	0.10	0.10	0.065	0.065	0.065
	Parametric	0.40	0.40	0.25	0.25	0.25
	Visual/Mechanical	0.25	0.25	0.15	0.15	0.10
Linear	Electrical Inoperative	0.25	0.15	0.15	0.15	0.10
	Parametric	0.65	0.40	0.40	0.40	0.25
	Visual/Mechanical	0.15	0.15	0.15	0.15	0.15
Power Transistors	Electrical Inoperative	0.10	0.10	0.10	0.10	0.10
	Parametric	0.40	0.40	0.40	0.40	0.25
	Visual/Mechanical	0.25	0.25	0.25	0.15	0.15
Small Signal Transistors	Electrical Inoperative	0.15	0.15	0.10	0.10	0.10
	Parametric	0.65	0.65	0.40	0.40	0.40
	Visual/Mechanical	0.40	0.40	0.25	0.15	0.15
CMOS	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15
MOS Microprocessors	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15
NMOS Memories	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15
LS TTL ECL	Function/Parametric	0.15	0.15	0.065	0.065	0.065
Bipolar Memory/LSI	Visual/Mechanical	0.65	0.15	0.065	0.065	0.065
ALS/FAST	Function/Parametric	–	–	–	0.065	0.065
	Visual/Mechanical					

EVOLUTION OF AVERAGE OUTGOING QUALITY – A.O.Q.
(TOTAL A.O.Q. INCLUDING VISUAL, MECHANICAL AND ELECTRICAL)



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OUTGOING QUALITY

Although test procedures may vary from product to product within Motorola, the same philosophy applies when considering quality objectives. Motorola's mission is to be a Quality and Reliability leader worldwide.

HIGHLIGHTS:

Motorola recognizes that you, our customers, are truly concerned about improving your own quality image. You are, therefore, concerned about the quality of the product Motorola supplies you.

Our customers measure us by the level of defects in the products we supply at incoming inspection, during assembly and, most important, field reliability.

During the past years, Motorola has achieved impressive reductions in defect rates known as A.O.Q. or Average Outgoing Quality. Instrumental in this success has been the planned continuous reduction in outgoing A.Q.L. to a point where Motorola believes that over all products it can demonstrate the most aggressive A.Q.L.'s in the industry.

This aggressive program has been designed to help eliminate expensive incoming inspection at our customers.

All of the facilities also practice an extremely demanding parts per million program program (PPM).

The PPM performance of all Motorola products is calculated in each location using the same method; they are, therefore, directly comparable. Motorola is well aware that when discussing PPM with existing or potential customers, it is of paramount importance to explain exactly which failure categories are included in the stated PPM figures. Motorola's PPM figures will include:

- Electrical Inoperative Failure
- Electrical Parametric Failures (dc and ac)
- Visual and Mechanical criteria.

In many published cases, stated PPM values refer to Electrical Inoperative failures only.

At Motorola, the Electrical Inoperative, the Electrical Parametric and the Visual/Mechanical failure rates are calculated separately and then combined to reach an overall total. In this way Motorola believes that is giving its customers a true and accurate assessment of the quality of the product. Unqualified PPM statements can be misleading and cause the customer to expect quality levels which cannot be achieved. For example, Motorola MOS Logic A.O.Q. is separated into Electrical Inoperative/Electrical Parametric (280 PPM) and Visual/Mechanical (486 PPM). Other product families such as Small Signal Plastic Transistors are already reaching 50 PPM in Electrical Inoperative failure rate.

The Motorola PPM graphs are excellent examples of what has been achieved over the last years with regard to quality improvements.

Reductions between 50% and 300% in average outgoing quality are typical across the broad range of Motorola products.

Throughout the semiconductor industry there have been, and there still are, examples of manufacturers offering higher quality standards at a premium. This is **not** a Motorola strategy, we believe that our customers should expect high quality products at no extra cost. This is Motorola's aim and we will continue to aggressively pursue Quality and Reliability improvements which will be passed on to our customers as an obligation on our part.

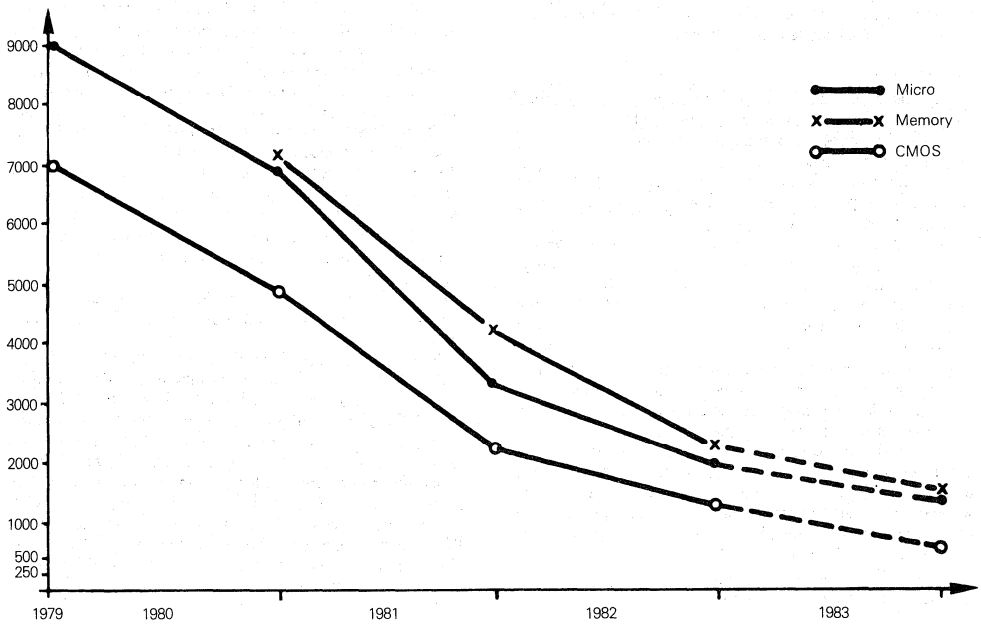
Also, we actively encourage our customers to provide their quality results at their Incoming Inspection, during their manufacturing process and from the field in order to better correlate and further improve our quality performance.

MOTOROLA A.O.Q. PLAN

	History Average			Dec	Goal
	1980	1981	1982	1982	1983
Power Transistors	3400	1400	1100	950	700
Rectifiers	1750	1100	1000	950	700
Small Signal Metal	4100	2200	1400	1100	800
Small Signal Plastic	1500	1200	1030	800	600
Linear I/C's	4300	2800	1900	2000	1000
L. and S.F.	5000	2370	1380	1150	500
Memory	7000	4360	2400	2900	1300
Microprocessor	7000	3860	2450	2900	1300
Bipolar Digital Logic	1260	802	975	800	500
Bipolar Memory/LSI	1620	1200	1000	151	700

A.O.Q. Includes all Defects: Visual, Mechanical, Electrical Inoperative and Parametric.

AVERAGE A.O.Q. IN P.P.M. FOR MOS PRODUCTS FIGURES
INCLUDE FUNCTIONAL/PARAMETRIC/VISUAL/MECHANICAL



RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of Reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, useful life and wearout. When a device is produced, there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality, are reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occassional random failure mechanisms appear; the useful life typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using strictly controlled design techniques and selectivity in applications, this period is shifted well beyond the lifetime required by the user.

FIGURE 1

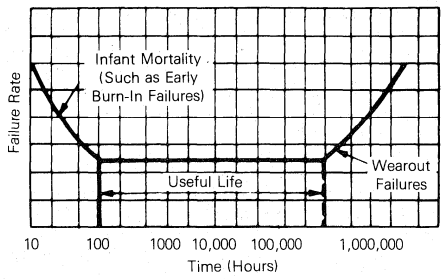
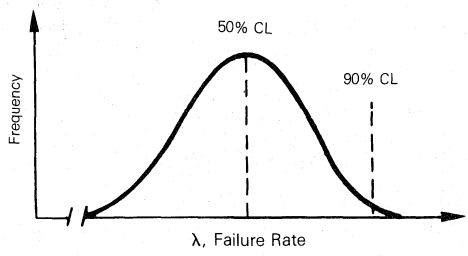


FIGURE 2



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Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P_o = e^{-\lambda t}$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures In Time= $(\%/10^3$ hrs) $\times 10^{-4} = 10^{-9}$ failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and λ is calculated using x^2 distribution through the equation:

$$\lambda \leq \frac{x^2\,(x,\ 2r+2)}{2nt}$$

$$\text{where } x = \frac{100 - CL}{100}$$

CL = Confidence Limit in percent
r = Number of rejects
n = Number of devices
t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r+ 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to x^2 tables.

The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the x^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate.

Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behaviour fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\Theta/kT}$$

where R(t) = Reaction rate as a function of time and temperature

R_0 = A constant
t = Time
Θ = Activation energy in electron volts
k = Boltzman's constant
T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form:

$$t = t_0 e^{\Theta/kT}$$

where t = time

t_0 = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by Θ. Θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by semiconductors varies from about 0.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does imply a high Θ. Studies by Bell Telephone Laboratories have indicated that an overall Θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in as specified in Method 1015 of MIL-STD-883. Data taken by Motorola on Integrated Circuits have verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3). For Discrete products, 0.7 eV is generally applied.

To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1.

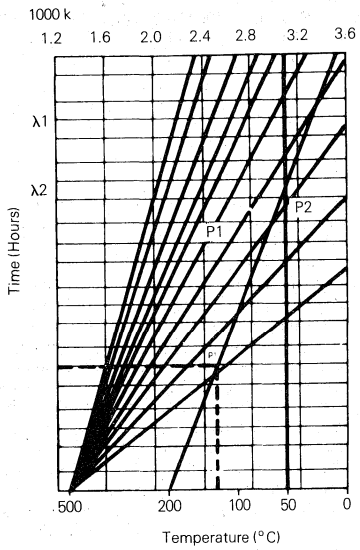
Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the x^2 formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 7.8 million hours results at a T2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1,000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.026%/1,000 hour failure rate, as illustrated in Figure 4.

Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted λ. A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Every device will eventually fail, but with the present techniques in Semiconductor design and applications, the wearout phase is extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The parameter

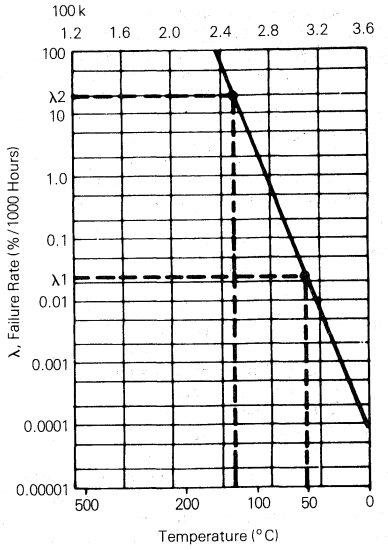
used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only few significant wearout mechanisms: electromigration of circuit metallization, electrolytic corrosion in plastic devices and metal fatigue for Power devices.

FIGURE 3
NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES



For increased flexibility in working with a broad range of device hours, the time-temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

FIGURE 4
FAILURE RATE



Reliability

RELIABILITY TESTS: DEFINITION, PURPOSE AND PROCEDURES

These definitions are intended to give the reader a brief understanding of the test currently used at Motorola for reliability checking. They also state which main failure mechanisms are accelerated by the test.

HIGH TEMPERATURE STORAGE LIFE

An environmental test where only temperature is the stress. Temperature and test duration must be specified. Usually temperature is the maximum storage temperature of the devices under test. Main failure mechanisms are metallization, bulk silicon, corrosion.

HIGH TEMPERATURE REVERSE BIAS (HTRB)

An environmental stress combined with an electrical stress whereby devices are subjected to an elevated temperature and simultaneously reverse biased. To be effective, voltage must be applied to the devices until they reach room temperature at the completion of the test. Temperature, time and voltage levels must be specified. Accelerated failure mechanisms are inversion, channeling, surface contamination, design.

HIGH HUMIDITY, HIGH TEMPERATURE REVERSE BIAS (H^3TRB)

A combined environmental/electrical stress whereby devices are subjected to an elevated ambient temperature and high humidity, simultaneously reverse biased for a period of time. Normally performed on a sample basis (qualification) on non-hermetic devices. The most common conditions is 85°C and 85% relative humidity. More extreme conditions generally are very destructive to the chambers used. Time, temperature, humidity and voltage must be specified. This accelerated test mainly detects corrosion risks.

STEADY STATE OPERATING LIFE

An electrical stress whereby devices are forward (reverse for zeners) biased at full rated power for prolonged duration. Test is normally 25°C ambient and power is 100% of full rated. (For power devices the I/C's maximum operating Ti is used.) Duration, power and ambient, if other than 25°C, must be specified. Accelerated failure mechanisms mainly are metallization, bulk silicon, oxide, inversion and channeling.

DYNAMIC OPERATING LIFE

An electrical stress whereby devices are alternately subjected to forward bias at full rated power or current and reverse bias.

Duration, power, duty cycle, reverse voltage ambient and frequency must be specified. Used normally for rectifiers and silicon controlled rectifiers. Failure mechanisms are essentially the same as steady state operating life.

INTERMITTENT OPERATING LIFE (POWER CYCLING)

An electrical stress whereby devices are turned on and off for a period of time. During the "on" time the devices are turned on at a power such that the junction temperature reaches its maximum rating. During "off" cycle the devices return to 25°C ambient. Duration, power, or duty cycle must be individually specified. Accelerated failures mechanisms are mainly die bonds, wire bond, metallization, bulk silicon, and oxide.

THERMAL SHOCK (TEMPERATURE CYCLING)

An environmental stress whereby devices are alternately subjected to a low and high temperature with or without a dwell time in between to stabilize the devices to 25°C ambient — the medium is usually air. Temperatures, dwell times and cycles must be specified. Failure mechanisms are essentially die bonds, wire bonds, and package.

THERMAL SHOCK (GLASS STRAIN)

An environmental stress whereby the devices are subjected to a low temperature, stabilized and immediately transferred to a high temperature. The medium is usually liquid. Failures mechanisms essentially are the same as temperature cycling.

EXAMPLE OF NEW PROCESS QUALIFICATION TESTS

Test	Condition	Duration	MIL-STD-883 Reference Test Method
Operating Life	125°C, 5 V or 15 V	1,000 Hours	1005
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours	
Autoclave	121°C, 100% R.H. 15P.S.I.G.	144 Hours	
High Temperature Storage	150°C	1,000 Hours	
Thermal Cycle (Air to Air)	−65°C to 150°C 5 Min Dwell	1,000 Cycles	1010
Thermal Shock (Liquid to Liquid)	−65°C to 150°C 5 Min Dwell	1,000 Cycles	1011
Shock, Vibration, and Constant Acceleration	1,500G, 3 per Axis 150–2,000 Hz, 20 g 30 kg	0.5 MS 2 Hours	2002 2007 2001
Data Retention Bake (Non Volation Memories)	200/250°C	1,000 Hours	

MECHANICAL SHOCK

A mechanical stress whereby the devices are subjected to high impact forces normally in two or more of the six orientations X1, Y1, Z1, X2, Y2, Z2. Tests are to verify the physical integrity of the devices. G forces, pulse duration, and number of shocks and axes must be specified.

VIBRATION VARIABLE FREQUENCY

Same as Vibration Fatigue except that frequency is logarithmically varied from 100 Hz to 1 kHz and back. Number of cycles is normally four. Cycle time, amplitude and total duration must be specified. Failure mechanisms are mainly package, wire bond – this test is not applicable to molded devices.

EXAMPLE OF NEW PACKAGE QUALIFICATION TESTS

Test	Condition	Duration	MIL-STD-883 Reference Test Method
Operating Life	125°C, 5 V or 15 V	1,000 Hours	1005
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours	
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	144 Hours	
High Temperature Storage	150°C	1,000 Hours	
Thermal Cycle (Air to Air)	−65°C to 150°C 5 Min Dwell	1,000 Cycles	1010
Thermal Shock (Liquid to Liquid)	−65°C to 150°C 5 Min Dwell	1,000 Cycles	1011
Shock, Vibration, and Constant Acceleration	1,500 G, 3 per Axis 150−2,000 Hz, 20 g 30 kg	0.5 ms 2 Hours	2002 2007 2001
Hermeticity	1.85, 10^{-8} atm cc/sec		1014
Visual Inspection			2008
Dimensions	Outline Dwg.		2016
Marking Permanency			2015
Solderability	230°C	3 Seconds	2003
Wire Bond Strength (Post Seal)	1.5 Gram		2011
Die Shear			2027

EXAMPLE OF STANDARD RELIABILITY PROGRAM

Reliability Engineering Department	Motorola Reliability Program For:			
Test Group	**Test**	**SS**	**Frequency**	**Test Methods/Conditions**
Reliability Audit	Thermal Shock	25	1 Product Line Per Week	MIL-STD-883, Method 1011 −25°C, +125°C. Dwell Time 5 mn, 100 Cycles
	High Temperature Reverse Bias	40		TA = 150°C, VCB = .8 VCB max. 168 hours
Life Tests	High Temperature Reverse Bias	25 (+2)	3 Product Lines Per Month	TA = 150°C, VCB = .8 VCB max. 1,000 hours
	High Temperature Storage	25 (+2)		TA = 150°C, 1,000 hours
	Steady State Life	25 (+2)		MIL-STD-883, Method 1005 TA = 125°C, 1,000 hours
	High Humidity	25		TA = 85°C, 85% Humidity
	High Temperature Reverse Bias	(+2)		VCB = .8 VCB max. 1,000 hours
(+2) devices for correlation purpose				

Product Family	Test Conditions	Device Hours	No. Of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Non Hermetic Interface I/C's	Operating T_j = 155°C	591,552	64	1 eV	70°C	0.014
Consumer I/C's	Operating T_j = 125°C	13,082,000	39	1 eV	70°C	0.0029
DO4/DO5 Rectifier	T_j = 150°C VR = .8 BVR	798,000	5	.7 eV	70°C	0.009
Plastic Axial Diodes	T_j = 100°C VR = .8 BVR	295,000	3	.7 eV	70°C	0.21
Button Diodes	T_j = 150°C VR = .8 BVR	520,000	5	.7 eV	70°C	0.014
Small Signal Plastic Transistor	T_j = 150°C VCB = .8 BVCO	579,000	6	.7 eV	70°C	0.014
Small Signal Metal Transistor	T_j = 150°C VCB = .8 BVCBO	3,944,000	12	.7 eV	70°C	0.0039
Case 77 Power Plastic Transistor	T_j = 150°C VBC = .8 BVCBO	364,416	2	.7 eV	70°C	0.0097
TO220 Power Plastic Transistor	T_j = 150°C VCB = .8 BVCBO	366,080	0	.7 eV	70°C	0.0028
TO3P Power Plastic Transistor	T_j = 150°C VCB = .8 BVCBO	297,024	3	.7 eV	70°C	0.016
TO3 Power Metal Transistor	T_j = 150°C VCB = .8 BVCBO	247,104	3	.7 eV	70°C	0.019

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
CMOS Ceramic	125°C Static Bias	6.5×10^7	11	1 EV	50°C 85°C	0.00074 0.025
CMOS Plastic	125°C Static Bias	2.1×10^8	17	1 EV	85°C	0.0088
6800 Series Plastic	125°C Dynamic Bias 5 V	2.88×10^6	47	1 EV	70°C	0.039
U.V. EPROM Life Test	125°C Dynamic Bias 5 V	434,456	3	1 EV	70°C	0.009
Data Retention	250°C Bake	519,120	3	0.7 EV	70°C	0.0075
EEPROM Life Test	125°C Dynamic Bias 5 V	917,280	25	1 EV	70°C	0.027
Data Retention	250°C	966,672	19	0.7 EV	70°C	0.020
64K DRAM	125°C Dynamic Bias 5.5 V	1.05×10^6	6	0.7 EV	70°C	0.028

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 90% Confidence
LS-TTL	125°C Static Basis −5.2 V			1.0 eV	70°C	0.0029
ECL	125°C Static Bias 5 V	61.74×10^6	7	1.0 eV	85°C	0.0189

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Operational Amplifier	Operating $T_j = 135°C$	437,472	2	1 eV	70°C	0.0026
Hermetic Interface I/C's	Operating $T_j = 135°C$	718,848	4	1 eV	70°C	0.0033

The reliability approach at Motorola Semiconductors is based on designing in reliability rather than testing for reliability only. This concept is reflected by Motorola's mandatory procedures which require product, process and packaging qualification on three independently produced lots before any product is released to volume production. Reliability engineering approval supported by an officially documented report is required before any product is released to manufacturing. Tests at both maximum rated and accelerated stress levels are performed. Acceleration is important to determine how and at what stress level a new design, product process or package would fail. This information provides an indication of what design changes can be implemented to ensure a wider and safer margin between the maximum rated stress condition and the devices stress limitation.

As well as qualifying all new products, processes and piece-parts, each Motorola manufacturing facility operates an ongoing reliability monitor which covers all process and packaging options. This program provides a continuous up-to-date data base which is summarized in periodical reports.

Reliability statistics supporting all Motorola Semiconductor devices can be obtained from any of the Motorola Sales Offices upon request. The present operating life test results demonstrates Motorola's reputation for producing semiconductors with reliability second to none.

The Quality organization in each facility is responsible for preparing and maintaining a Quality Manual which describes in detail the quality systems and associated Reliability and Quality Assurance organization, policies, and procedures. This manual must be appraised and ultimately approved by the appropriate approval authority.

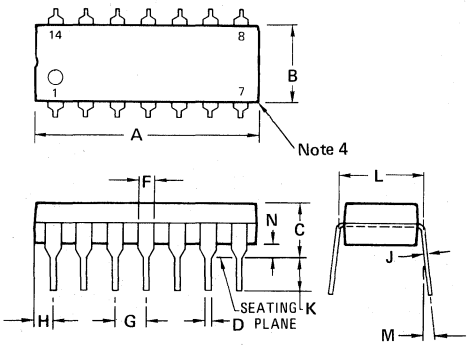
Package Dimensions

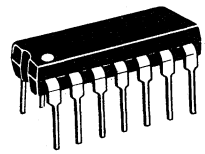
PACKAGE DIMENSIONS

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

14-PIN PACKAGE

PLASTIC PACKAGE
CASE 646-05



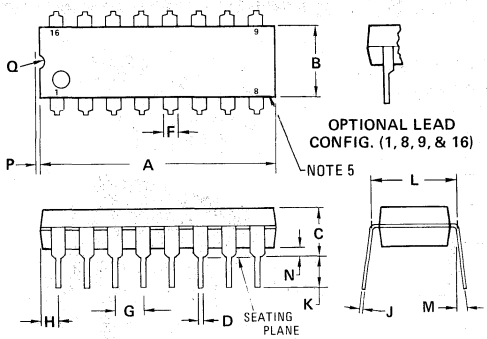


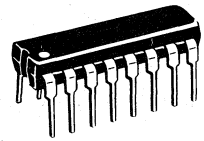
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

16-PIN PACKAGE

PLASTIC PACKAGE
CASE 648-05

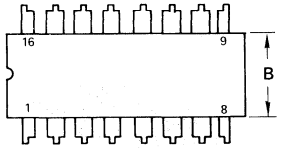


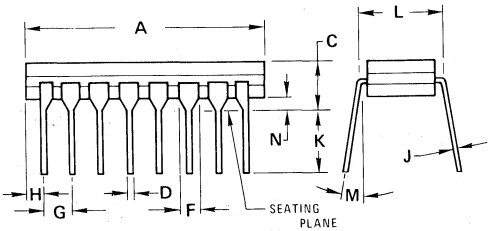


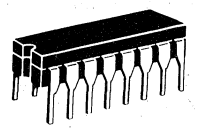
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

CERAMIC PACKAGE
CASE 620-08





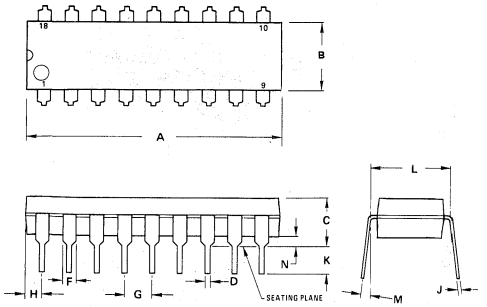


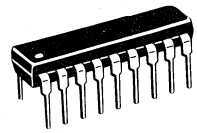
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

18-PIN PACKAGE

PLASTIC PACKAGE
CASE 707-02



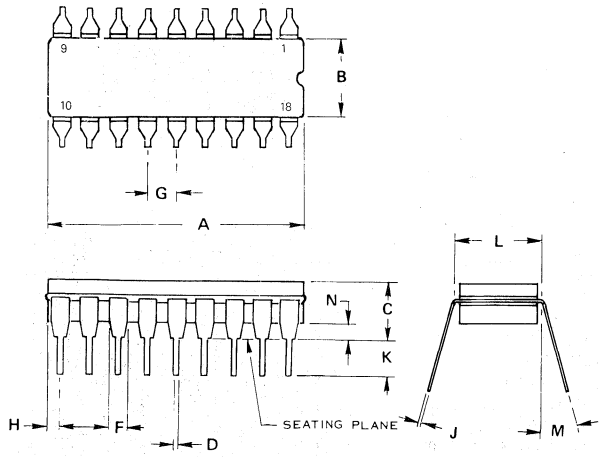


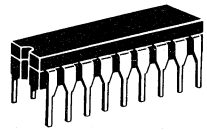
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CERAMIC PACKAGE
CASE 726-04





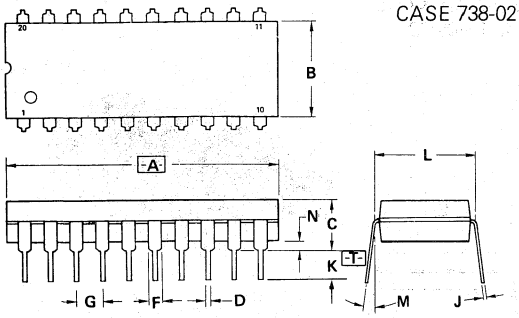
NOTES:

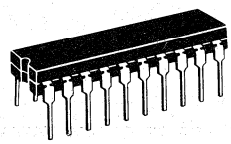
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

20-PIN PACKAGE

PLASTIC PACKAGE
CASE 738-02

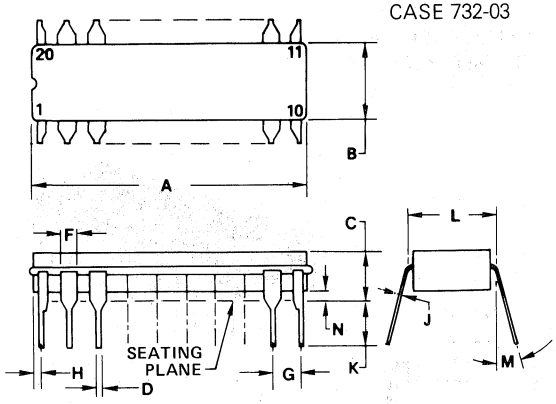


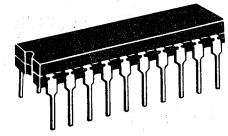


NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CERAMIC PACKAGE
CASE 732-03





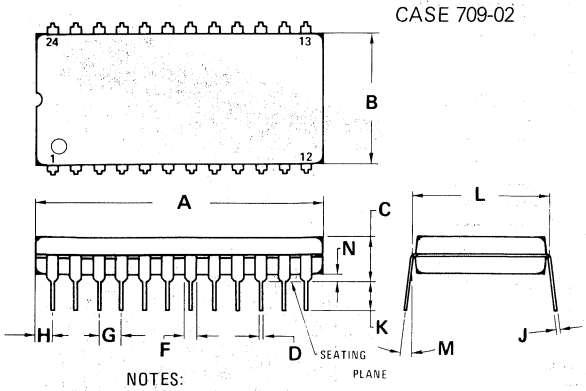
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

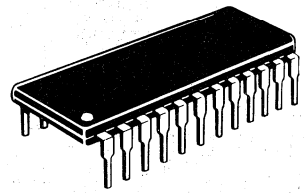
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

PLCC PACKAGE — SEE PAGE 11-9

24-PIN PACKAGE

PLASTIC PACKAGE
CASE 709-02

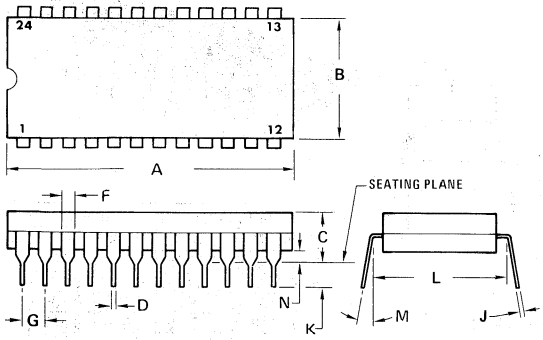


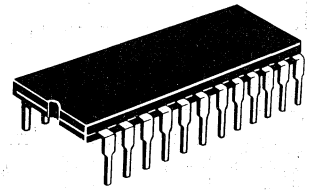


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERAMIC PACKAGE
CASE 623-05



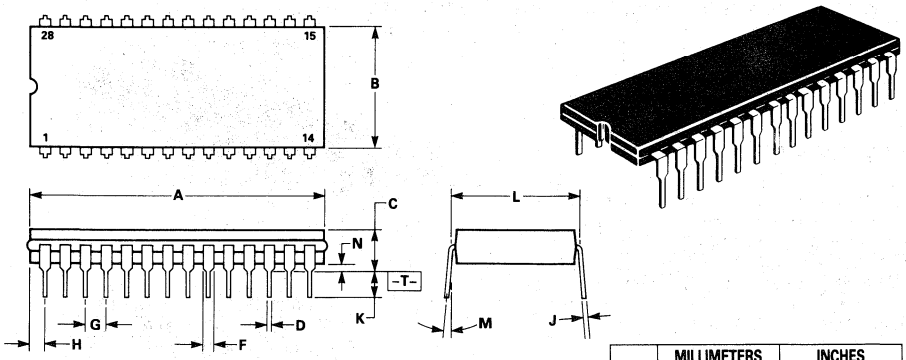


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

28-PIN PACKAGE

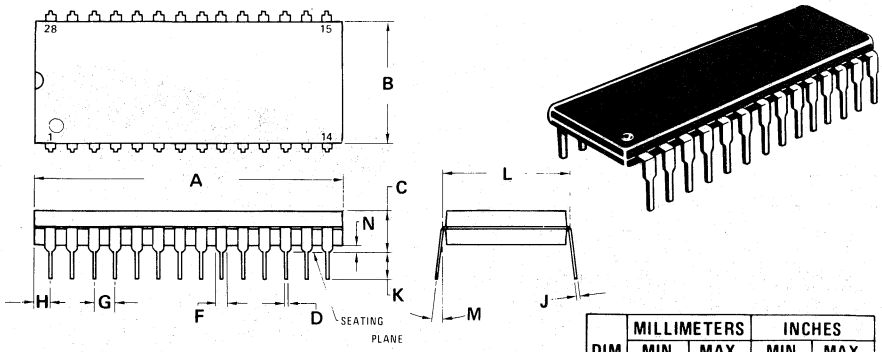
CERAMIC PACKAGE
CASE 733-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS: ⌖ ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

PLASTIC PACKAGE
CASE 710-02

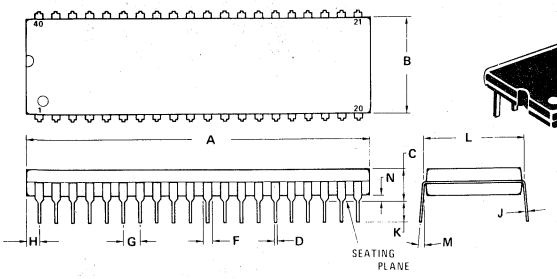


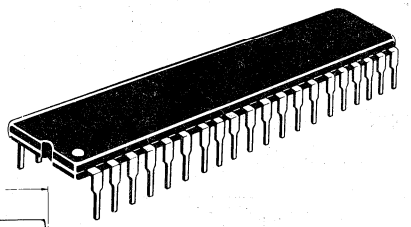
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

40-PIN PACKAGE

PLASTIC PACKAGE
CASE 711-03

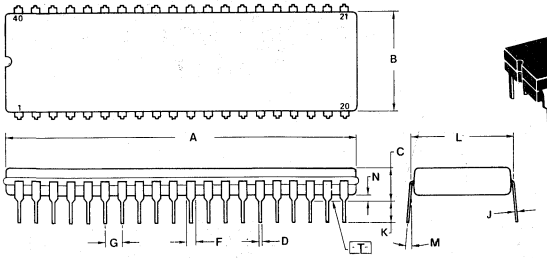


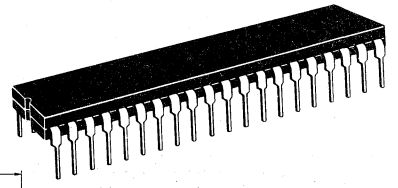


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERAMIC PACKAGE
CASE 734-04



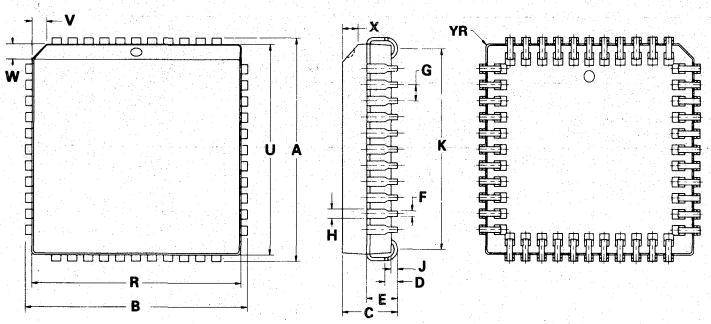


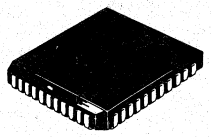
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5^0	15^0	5^0	15^0
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | Ø 0.25(0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

40-PIN PACKAGE

PLCC PACKAGE
CASE 777-01



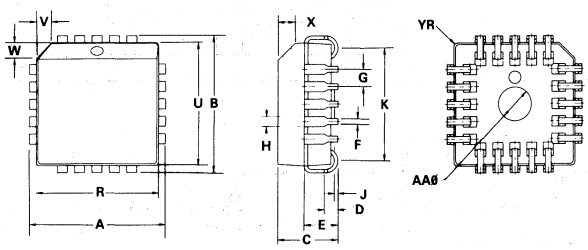


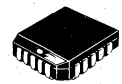
NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	14.99	16.00	0.590	0.630
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

20-PIN PACKAGE

PLCC PACKAGE
CASE 775-01





NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

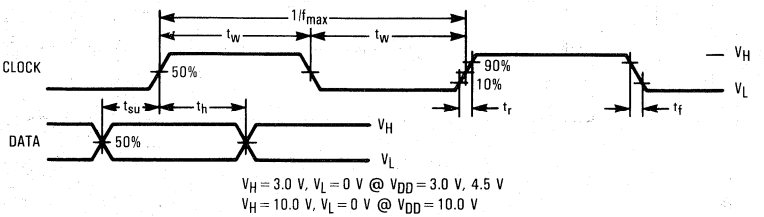
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.02	0.385	0.395
B	9.78	10.02	0.385	0.395
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.13	0.38	0.005	0.015
K	7.37	8.38	0.290	0.330
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020
AA	2.34	2.71	0.088	0.107

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		–	3.0 to 10.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data, Clock, BP In)		3.0 4.5 10.0	0.4 0.8 0.8	V
V_{IH}	Minimum High-Level Input Voltage (Data, Clock, BP In)		3.0 5.5 10.0	2.0 2.0 8.0	V
I_{OL}	Minimum Low-Level Output Current (BP Out) (Out 1 to Out 33)	$V_{out} = 0.3$ V	 3.0 3.0	 320 20	μA
I_{OH}	Minimum High-Level Output Current (BP Out) (Out 1 to Out 33)	$V_{out} = 2.7$ V	 3.0 3.0	 −320 −20	μA
V_{OO}	Average DC Output Offset Voltage (BP Out Relative to Out 1 through Out 33)	BP Out: $C_L = 8750$ pF Out 1 to 33: $C_L = 250$ pF	3.0 10.0	±50 ±50	mV
I_{in}	Maximum Input Leakage Current (Data, Clock, BP In)	$V_{in} = V_{DD}$ or V_{SS}	10.0	±1.0	μA
I_{DD}	Maximum Quiescent Supply Current (per Package)	Osc In: $V_{in} = V_{SS}$ BP In, Data, Clock: $V_{in} = V_{DD}$ or V_{SS} $I_{out} = 0$ μA	10.0	10	μA
I_{dd}	Maximum RMS Operating Supply Current (per Package)	$R_X = 1.0$ MΩ, $C_X = 470$ pF BP Out Tied to BP In Clock, Data: $V_{in} = V_{DD}$ or V_{SS} $I_{out} = 0$ μA	10.0	40	μA

AC ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, Input $t_r = t_f = 50$ ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figure 1)	3.0 4.5 10.0	400 850 1800	kHz
t_{su}	Minimum Setup Time, Data to Clock (Figure 1)	3.0 4.5 10.0	300 180 100	ns
t_h	Minimum Hold Time, Clock to Data (Figure 1)	3.0 4.5 10.0	300 130 50	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	3.0 4.5 10.0	1250 585 275	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	3.0 4.5 10.0	300 300 300	ns
C_{in}	Maximum Input Capacitance	–	10	pF



$V_H = 3.0$ V, $V_L = 0$ V @ $V_{DD} = 3.0$ V, 4.5 V
$V_H = 10.0$ V, $V_L = 0$ V @ $V_{DD} = 10.0$ V

Figure 1. Switching Waveforms

Continuation of data sheet MC145453 page 3

PIN DESCRIPTIONS

INPUTS

Data

Serial data input. Data on this pin is serially entered into the on-chip shift register on the rising edge of Clock. The data stream consists of a Start Bit (high), followed by 33 Display Bits, plus 2 Trailing Bits (don't cares). This device does not contain a decoder, which allows the flexibility of formatting the segment information externally. Display Bit 1 controls the LCD segment connected to Out 1, Bit 2 controls Out 2, etc. If a Display Bit is high, the associated segment is activated. The Display Bits are stored in latches which eliminates display flicker during shifting.

Clock

Each rising edge on Clock causes Data to be shifted into the 36-bit shift register. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode. Clock need not be synchronous to Osc In nor BP In. The internal load shown in Figure 2 transfers the 33 Display Bits to the on-chip latches. The internal reset clears the shift register (only) to ready the device for the next set of data.

BP In

Backplane in. The signal applied to this input must also be tied to the backplane of the LCD. BP In is the common input to the 33 gated drivers, and may be sourced from the on-chip oscillator output, BP Out. (See Figure 3.) To reduce interference from the display driver in analog designs, BP In may be synchronized with a system clock. The BP In waveform must be a 50% duty cycle to minimize offset voltage to the LCD which impacts display lifetime. (See Figures 4 and 5.) The BP In frequency should be 25 to 250 Hz, depending on the display.

Osc In

Oscillator input. As shown in Figure 3, this pin is used in conjunction with an external resistor and capacitor to form an oscillator. The oscillator frequency is divided by 16 and appears at BP Out. With a 5 V supply, nominal values of 1 MΩ and 470 pF produce a 60 to 150 Hz waveform at BP Out. If the on-chip oscillator is not used, Osc In must be tied to V_{SS} which minimizes power consumption and insures reliable chip operation.

OUTPUTS

BP Out

Backplane output. This pin may be used to provide a 50% duty cycle waveform to directly drive the backplane of the LCD and BP In. (See Figure 3.) If the on-chip oscillator is not used, BP Out must be left unconnected. (See Figure 4.) When paralleling devices, BP Out fans out to drive the BP In pins of other packages. (See Figure 6.)

Out 1 through Out 33

Frontplane driver outputs which are tied directly to the LCD.

POWER

V_{SS}

Most negative supply potential. This pin is usually ground.

V_{DD}

Most positive supply potential. This voltage may range from 3 to 10 volts with respect to V_{SS}.

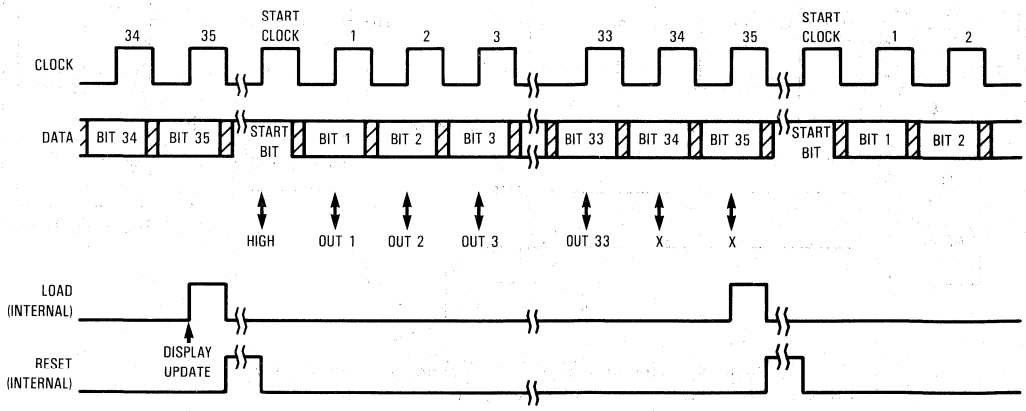


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

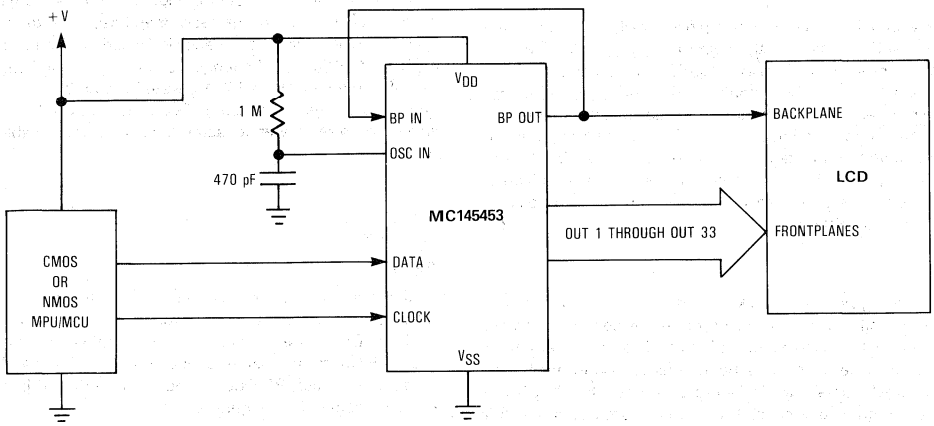


Figure 3. Using On-Chip Oscillator

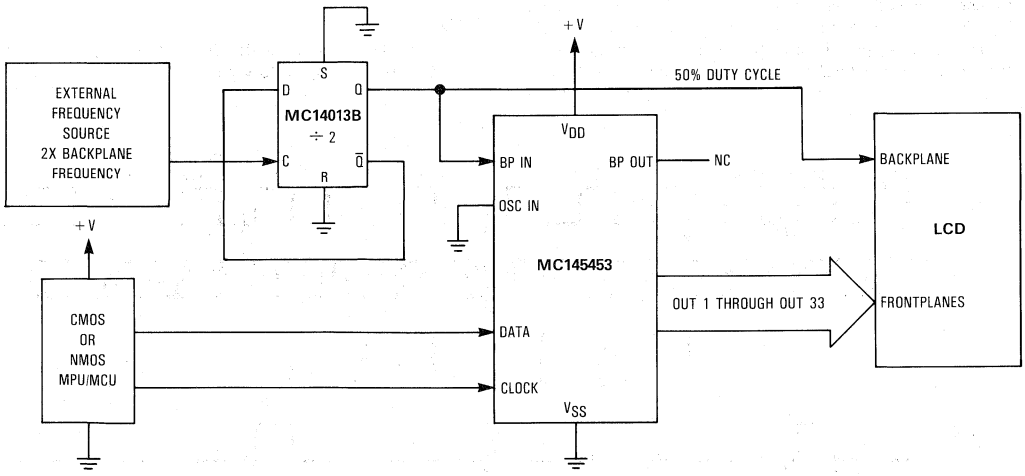


Figure 4. Converting External Backplane Frequency Source to 50% Duty Cycle

APPLICATIONS INFORMATION (CONT'D)

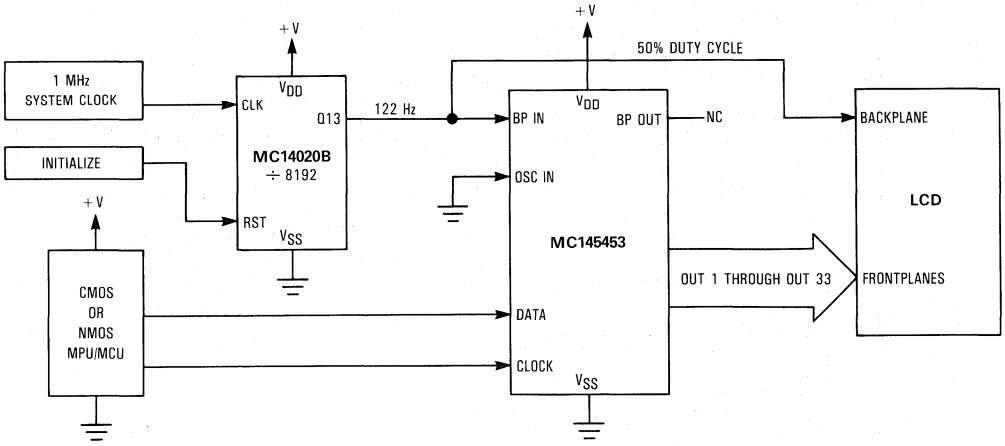


Figure 5. Using Low-Cost Divider to Sync Backplane Frequency

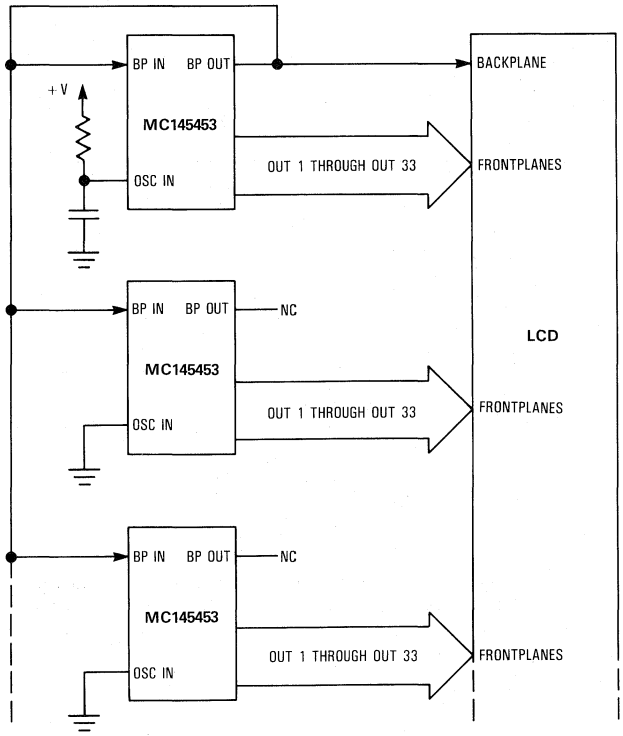


Figure 6. Paralleling Devices to Increase Number of Driven Segments

Continuation of data sheet MC145453 page 6

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